

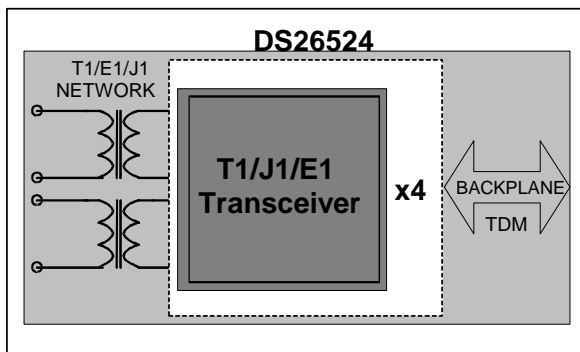
GENERAL DESCRIPTION

The DS26524 is a single-chip 4-port framer and line interface unit (LIU) combination for T1, E1, and J1 applications. Each channel is independently configurable, supporting both long-haul and short-haul lines.

APPLICATIONS

Routers
Channel Service Units (CSUs)
Data Service Units (DSUs)
Muxes
Switches
Channel Banks
T1/E1 Test Equipment

TYPICAL OPERATING CIRCUIT



ORDERING INFORMATION

| PART | TEMP RANGE | PIN-PACKAGE |
|------------|----------------|--------------|
| DS26524G | 0°C to +70°C | 256 TE-CSBGA |
| DS26524G+ | 0°C to +70°C | 256 TE-CSBGA |
| DS26524GN | -40°C to +85°C | 256 TE-CSBGA |
| DS26524GN+ | -40°C to +85°C | 256 TE-CSBGA |

+ Denotes lead-free/RoHS compliant device.

FEATURES

- Four Complete T1, E1, or J1 Long-Haul/Short-Haul Transceivers (LIU plus Framer)
- Independent T1, E1, or J1 Selections for Each Transceiver
- Internal Software-Selectable Transmit- and Receive-Side Termination for 100Ω T1 Twisted Pair, 110Ω J1 Twisted Pair, 120Ω E1 Twisted Pair, and 75Ω E1 Coaxial Applications
- Crystal-Less Jitter Attenuator can be Selected for Transmit or Receive Path; Jitter Attenuator Meets ETS CTR 12/13, ITU-T G.736, G.742, G.823, and AT&T Pub 62411
- External Master Clock can be Multiple of 2.048MHz or 1.544MHz for T1/J1 or E1 Operation; This Clock is Internally Adapted for T1 or E1 Usage in the Host Mode
- Receive-Signal Level Indication from -2.5dB to -36dB in T1 Mode and -2.5dB to -44dB in E1 Mode in Approximate 2.5dB Increments
- Transmit Open- and Short-Circuit Detection
- LIU LOS in Accordance with G.775, ETS 300 233, and T1.231
- Transmit Synchronizer
- Flexible Signaling Extraction and Insertion Using Either the System Interface or Microprocessor Port
- Alarm Detection and Insertion
- T1 Framing Formats of D4, SLC-96, and ESF
- J1 Support
- E1 G.704 and CRC-4 Multiframe
- T1-to-E1 Conversion

Features Continued in Section 2.

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1. DETAILED DESCRIPTION

The DS26524 is a 4-port monolithic device featuring independent transceivers that can be software configured for T1, E1, or J1 operation. Each transceiver is composed of a line interface unit, framer, HDLC controller, elastic store, and a TDM backplane interface. The DS26524 is controlled via an 8-bit parallel port. Internal impedance matching is provided for both transmit and receive paths, reducing external component count.

The LIU is composed of a transmit interface, receive interface, and a jitter attenuator. The transmit interface is responsible for generating the necessary waveshapes for driving the network and providing the correct source impedance depending on the type of media used. T1 waveform generation includes DSX-1 line build-outs as well as CSU line build-outs of 0dB, -7.5dB, -15dB, and -22.5dB. E1 waveform generation includes G.703 waveshapes for both 75Ω coax and 120Ω twisted cables. The receive interface provides network termination and recovers clock and data from the network. The receive sensitivity adjusts automatically to the incoming signal level and can be programmed for 0dB to -43dB or 0dB to -12dB for E1 applications and 0dB to -15dB or 0dB to -36dB for T1 applications. The jitter attenuator removes phase jitter from the transmitted or received signal. The crystal-less jitter attenuator requires only a T1 or E1 clock rate, or multiple thereof, for both E1 and T1 applications, and can be placed in either transmit or receive data paths.

On the transmit side, clock, data, and frame-sync signals are provided to the framer by the backplane interface section. The framer inserts the appropriate synchronization framing patterns, alarm information, calculates and inserts the CRC codes, and provides the B8ZS/HDB3 (zero code suppression) and AMI line coding. The receive-side framer decodes AMI, B8ZS, and HDB3 line coding, synchronizes to the data stream, reports alarm information, counts framing/coding/CRC errors, and provides clock, data, and frame-sync signals to the backplane interface section.

Both transmit and receive paths have access to an HDLC controller. The HDLC controller transmits and receives data via the framer block. The HDLC controller can be assigned to any time slot, a portion of a time slot, or to FDL (T1) or Sa bits (E1). Each controller has 64-byte FIFOs, reducing the amount of processor overhead required to manage the flow of data.

The backplane interface provides a versatile method of sending and receiving data from the host system. Elastic stores provide a method for interfacing to asynchronous systems, converting from a T1/E1 network to a 2.048MHz, 4.096MHz, 8.192MHz, 16.384MHz, or N x 64kHz system backplane. The elastic stores also manage slip conditions (asynchronous interface). The interleave bus option (IBO) is provided to allow up to eight transceivers to share a high-speed backplane. The DS26524 also contains an internal clock adapter useful for the creation of a synchronous, high-frequency backplane timing source.

The parallel port provides access for configuration and status of all the DS26524's features. Diagnostic capabilities include loopbacks, PRBS pattern generation/detection, and 16-bit loop-up and loop-down code generation and detection.

1.1 Major Operating Modes

The DS26524 has two major modes of operation: T1 mode and E1 mode. The mode of operation for the LIU is configured in the LIU Transmit Receive Control register ([LTRCR](#)). The mode of operation for the framer is configured in the Transmit Master Mode register ([TMMR](#)). J1 operation is a special case of T1 operating mode.

2. FEATURE HIGHLIGHTS

2.1 General

- Member of the TEX-series transceiver family of devices. Software compatible with the DS26521 single, DS26522 dual, and DS26528 octal transceivers
- 256-pin TE-CSBGA package (17mm x 17mm, 1.00mm pitch)
- 3.3V supply with 5V tolerant inputs and outputs
- IEEE 1149.1 JTAG boundary scan
- Development support includes evaluation kit, driver source code, and reference designs

2.2 Line Interface

- Requires a single master clock (MCLK) for both E1 and T1 operation. Master clock can be 1.544MHz, 2.048MHz, 3.088MHz, 4.096MHz, 6.276MHz, 8.192MHz, 12.552MHz, or 16.384MHz
- Fully software configurable
- Short- and long-haul applications
- Ranges include 0dB to -43dB, 0dB to -30dB, 0dB to 20dB, and 0dB to -12dB for E1; 0dB to -36dB, 0dB to 30dB, 0dB to 20dB, and 0dB to -15dB for T1
- Receiver signal level indication from -2.5dB to -36dB in T1 mode and -2.5dB to -44dB in E1 mode in 2.5dB increments
- Internal receive termination option for 75 Ω , 100 Ω , 110 Ω , and 120 Ω lines
- Monitor application gain settings of 14dB, 20dB, 26dB, and 32dB
- G.703 receive synchronization signal mode
- Flexible transmit waveform generation
- T1 DSX-1 line build-outs
- T1 CSU line build-outs of 0dB, -7.5dB, -15dB, and -22.5dB
- E1 waveforms include G.703 waveshapes for both 75 Ω coax and 120 Ω twisted cables
- Analog loss-of-signal detection
- AIS generation independent of loopbacks
- Alternating ones and zeros generation
- Receiver power-down
- Transmitter power-down
- Transmitter short-circuit limiter with current-limit-exceeded indication
- Transmit open-circuit-detected indication

2.3 Clock Synthesizer

- Output frequencies include 2.048MHz, 4.096MHz, 8.192MHz, and 16.384MHz
- Derived from user-selected recovered receive clock

2.4 Jitter Attenuator

- 32-bit or 128-bit crystal-less jitter attenuator
- Requires only a 1.544MHz or 2.048MHz master clock or multiple thereof, for both E1 and T1 operation
- Can be placed in either the receive or transmit path or disabled
- Limit trip indication

2.5 Framer/Formatter

- Fully independent transmit and receive functionality
- Full receive and transmit path transparency
- T1 framing formats D4 and ESF per T1.403, and expanded SLC-96 support (TR-TSY-008)
- E1 FAS framing and CRC-4 multiframe per G.704, G.706, and G.732 CAS multiframe
- Transmit-side synchronizer
- Transmit midpath CRC recalculate (E1)

- Detailed alarm and status reporting with optional interrupt support
- Large path and line error counters
 - T1: BPV, CV, CRC-6, and framing bit errors
 - E1: BPV, CV, CRC-4, E-bit, and frame alignment errors
 - Timed or manual update modes
- DS1 Idle Code Generation on a per-channel basis in both transmit and receive paths
 - User defined
 - Digital Milliwatt
- ANSI T1.403-1999 support
- G.965 V5.2 link detect
- Ability to monitor one DS0 channel in both the transmit and receive paths
- In-band repeating pattern generators and detectors
 - Three independent generators and detectors
 - Patterns from 1 to 8 bits or 16 bits in length
- Bit-oriented code (BOC) support
- Flexible signaling support
 - Software or hardware based
 - Interrupt generated on change of signaling data
 - Optional receive-signaling freeze on loss of frame, loss of signal, or frame slip
 - Hardware pins provided to indicate loss of frame (LOF), loss of signal (LOS), loss of transmit clock (LOTIC), or signaling freeze condition
- Automatic RAI generation to ETS 300 011 specifications
- RAI-CI and AIS-CI support
- Expanded access to Sa and Si bits
- Option to extend carrier loss criteria to a 1ms period as per ETS 300 233
- Japanese J1 support
- Ability to calculate and check CRC-6 according to the Japanese standard
- Ability to generate Yellow Alarm according to the Japanese standard
- T1-to-E1 conversion

2.6 System Interface

- Independent two-frame receive and transmit elastic stores
- Independent control and clocking
- Controlled slip capability with status
- Minimum delay mode supported
- Flexible TDM backplane supports bus rates from 1.544MHz to 16.384MHz
- Supports T1 to CEPT (E1) conversion
- Programmable output clocks for fractional T1, E1, H0, and H12 applications
- Interleaving PCM bus operation
- Hardware signaling capability
- Receive-signaling reinsertion to a backplane multiframe sync
- Availability of signaling in a separate PCM data stream
- Signaling freezing
- Ability to pass the T1 F-bit position through the elastic stores in the 2.048MHz backplane mode
- User-selectable synthesized clock output

2.7 HDLC Controllers

- One HDLC controller engine for each T1/E1 port
- Independent 64-byte Rx and Tx buffers with interrupt support
- Access FDL, Sa, or single DS0 channel
- Compatible with polled or interrupt driven environments

2.8 Test and Diagnostics

- IEEE 1149.1 support
- Per-channel programmable on-chip bit error-rate testing (BERT)
- Pseudorandom patterns including QRSS
- User-defined repetitive patterns
- Daly pattern
- Error insertion single and continuous
- Total-bit and errored-bit counts
- Payload error insertion
- Error insertion in the payload portion of the T1 frame in the transmit path
- Errors can be inserted over the entire frame or selected channels
- Insertion options include continuous and absolute number with selectable insertion rates
- F-bit corruption for line testing
- Loopbacks (remote, local, analog, and per-channel loopback)

2.9 Control Port

- 8-bit parallel control port
- Intel or Motorola nonmultiplexed support
- Flexible status registers support polled, interrupt, or hybrid program environments
- Software reset supported
- Hardware reset pin
- Software access to device ID and silicon revision

3. APPLICATIONS

The DS26524 is useful in applications such as:

- Routers
- Channel Service Units (CSUs)
- Data Service Units (DSUs)
- Muxes
- Switches
- Channel Banks
- T1/E1 Test Equipment

4. SPECIFICATIONS COMPLIANCE

The DS26524 LIU meets all the latest relevant telecommunications specifications. [Table 4-1](#) and [Table 4-2](#) provide the T1 and E1 specifications and relevant sections that are applicable to the DS26524.

Table 4-1. T1-Related Telecommunications Specifications

| |
|--|
| ANSI T1.102: Digital Hierarchy Electrical Interface |
| AMI Coding |
| B8ZS Substitution Definition |
| DS1 Electrical Interface. Line rate ± 32 ppm; Pulse Amplitude between 2.4V to 3.6V peak; power level between 12.6dBm to 17.9dBm. The T1 pulse mask is provided that we comply. DSX-1 for cross connects the return loss is greater than -26dB. The DSX-1 cable is restricted up to 655 feet. |
| This specification also provides cable characteristics of DSX-Cross Connect cable—22 AVG cables of 1000 feet. |
| ANSI T1.231: Digital Hierarchy—Layer 1 in Service Performance Monitoring |
| BPV Error Definition; Excessive Zero Definition; LOS description; AIS definition. |
| ANSI T1.403: Network and Customer Installation Interface—DS1 Electrical Interface |
| Description of the Measurement of the T1 Characteristics—100 Ω . Pulse shape and template compliance according to T1.102; power level 12.4dBm to 19.7dBm when all ones are transmitted. |
| LBO for the Customer Interface (CI) is specified as 0dB, -7.5dB, and -15dB. Line rate is ± 32 ppm. Pulse Amplitude is 2.4V to 3.6V. |
| AIS generation as unframed all ones is defined. |
| The total cable attenuation is defined as 22dB. The DS26524 functions with up to -36dB cable loss. |
| Note that the pulse template defined by T1.403 and T1.102 are different, specifically at Times 0.61, -0.27, -34, and 0.77. The DS26524 is compliant to both templates. |
| Pub 62411 |
| This specification has tighter jitter tolerance and transfer characteristics than other specifications. The jitter transfer characteristics are tighter than G.736 and jitter tolerance is tighter the G.823. |
| (ANSI) “Digital Hierarchy—Electrical Interfaces” |
| (ANSI) “Digital Hierarchy—Formats Specification” |
| (ANSI) “Digital Hierarchy—Layer 1 In-Service Digital Transmission Performance Monitoring” |
| (ANSI) “Network and Customer Installation Interfaces—DS1 Electrical Interface” |
| (AT&T) “Requirements for Interfacing Digital Terminal Equipment to Services Employing the Extended Super Frame Format” |
| (AT&T) “High Capacity Digital Service Channel Interface Specification” |
| (TTC) “Frame Structures on Primary and Secondary Hierarchical Digital Interfaces” |
| (TTC) “ISDN Primary Rate User-Network Interface Layer 1 Specification” |

Table 4-2. E1-Related Telecommunications Specifications

| |
|--|
| ITU-T G.703 Physical/Electrical Characteristics of G.703 Hierarchical Digital Interfaces |
| Defines the 2048kbps bit rate—2048 \pm 50ppm; the transmission media are 75 Ω coax or 120 Ω twisted pair; peak-to-peak space voltage is \pm 0.237V; nominal pulse width is 244ns. |
| Return loss 51Hz to 102Hz is 6dB, 102Hz to 3072Hz is 8dB, 2048Hz to 3072Hz is 14dB. |
| Nominal peak voltage is 2.37V for coax and 3V for twisted pair. |
| The pulse template for E1 is defined in G.703. |
| ITU-T G.736 Characteristics of Synchronous Digital Multiplex Equipment Operating at 2048kbps |
| The peak-to-peak jitter at 2048kbps must be less than 0.05UI at 20Hz to 100Hz. |
| Jitter transfer between 2.048 synchronization signal and 2.048 transmission signal is provided. |
| ITU-T G.742 Second-Order Digital Multiplex Equipment Operating at 8448kbps |
| The DS26524 jitter attenuator is compliant with jitter transfer curve for sinusoidal jitter input. |
| ITU-T G.772 |
| This specification provides the method for using receiver for transceiver 0 as a monitor for the remaining seven transmitter/receiver combinations. |
| ITU-T G.775 |
| An LOS detection criterion is defined. |
| ITU-T G.823 The control of jitter and wander within digital networks that are based on 2.048kbps hierarchy. |
| G.823 Provides the jitter amplitude tolerance at different frequencies, specifically 20Hz, 2.4kHz, 18kHz, and 100kHz. |
| ETS 300 233 |
| This specification provides LOS and AIS signal criteria for E1 mode. |
| Pub 62411 |
| This specification has tighter jitter tolerance and transfer characteristics than other specifications. The jitter transfer characteristics are tighter than G.736 and jitter tolerance is tighter than G.823. |
| (ITU-T) "Synchronous Frame Structures used at 1544, 6312, 2048, 8488, and 44736kbps Hierarchical Levels" |
| (ITU-T) "Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704" |
| (ITU-T) "Characteristics of Primary PCM Multiplex Equipment Operating at 2048kbps" |
| (ITU-T) Characteristics of a Synchronous Digital Multiplex Equipment Operating at 2048kbps" |
| (ITU-T) "Loss Of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria" |
| (ITU-T) "The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048kbps Hierarchy" |
| (ITU-T) "Primary Rate User-Network Interface—Layer 1 Specification" |
| (ITU-T) "Error Performance Measuring Equipment Operating at the Primary Rate and Above" |
| (ITU-T) "In-Service Code Violation Monitors for Digital Systems" |
| (ETS) "Integrated Services Digital Network (ISDN); Primary Rate User-Network Interface (UNI); Part 1/Layer 1 Specification" |
| (ETS) "Transmission and Multiplexing; Physical/Electrical Characteristics of Hierarchical Digital Interfaces for Equipment Using the 2048kbps-Based Plesiochronous or Synchronous Digital Hierarchies" |
| (ETS) "Integrated Services Digital Network (ISDN); Access Digital Section for ISDN Primary Rate" |
| (ETS) "Integrated Services Digital Network (ISDN); Attachment Requirements for Terminal Equipment to Connect to an ISDN Using ISDN Primary Rate Access" |
| (ETS) "Business Telecommunications (BT); Open Network Provision (ONP) Technical Requirements; 2048kbps Digital Unstructured Leased Lines (D2048U) Attachment Requirements for Terminal Equipment Interface" |
| (ETS) "Business Telecommunications (BTC); 2048kbps Digital Structured Leased Lines (D2048S); Attachment Requirements for Terminal Equipment Interface" |
| (ITU-T) "Synchronous Frame Structures Used at 1544, 6312, 2048, 8488, and 44736kbps Hierarchical Levels" |
| (ITU-T) "Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704" |

5. ACRONYMS AND GLOSSARY

This data sheet assumes a particular nomenclature of the T1 and E1 operating environment. In each 125 μ s T1 frame, there are 24 8-bit channels plus a framing bit. It is assumed that the framing bit is sent first followed by channel 1. For T1 and E1, each channel is made up of 8 bits, which are numbered 1 to 8. Bit 1, the MSB, is transmitted first. Bit 8, the LSB, is transmitted last.

Locked refers to two clock signals that are phase- or frequency-locked or derived from a common clock (i.e., a 1.544MHz clock can be locked to a 2.048MHz clock if they share the same 8kHz component).

Table 5-1. Time Slot Numbering Schemes

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| TS | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
| Channel | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
| Phone Channel | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 |

6. BLOCK DIAGRAMS

Figure 6-1. Block Diagram

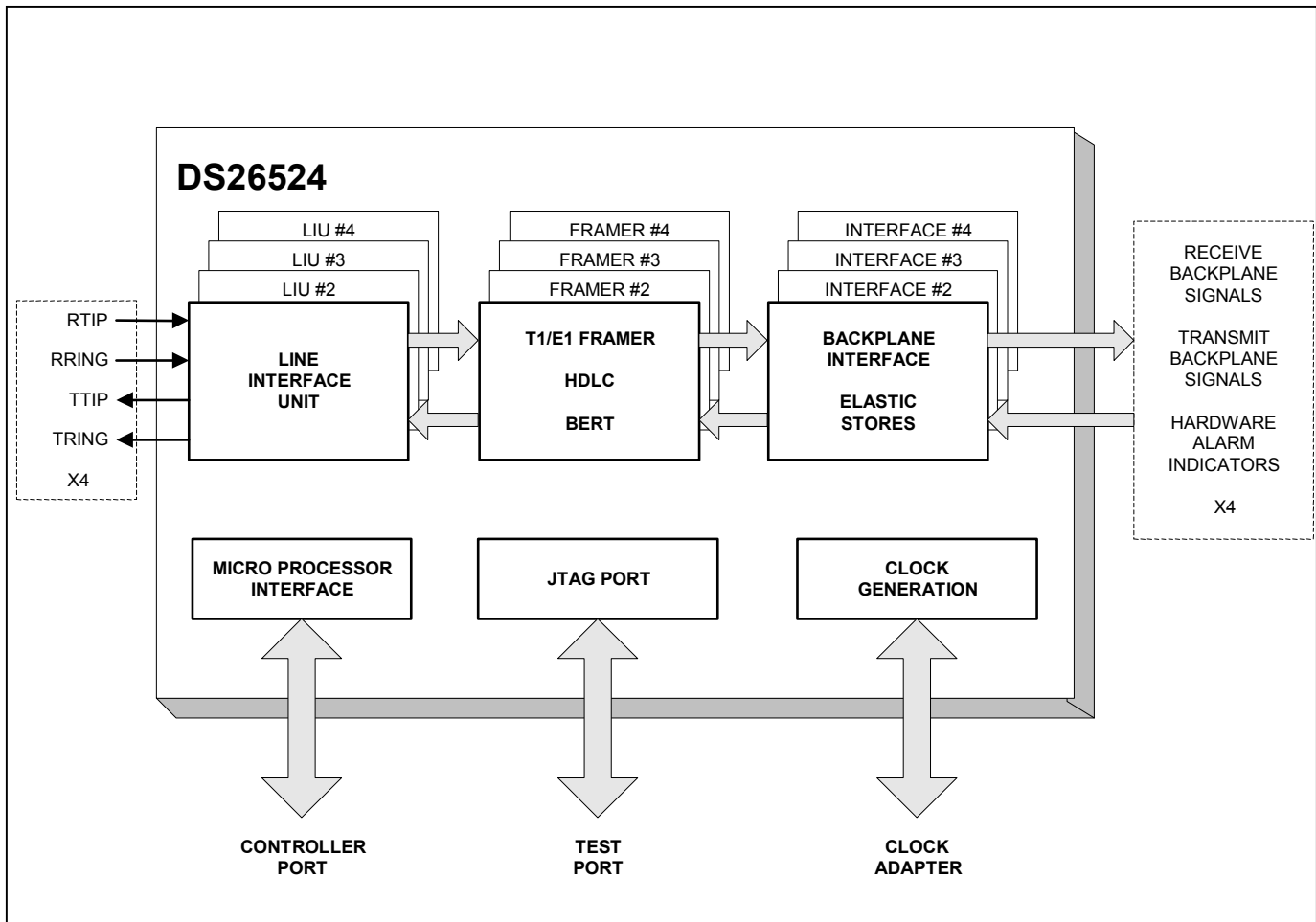
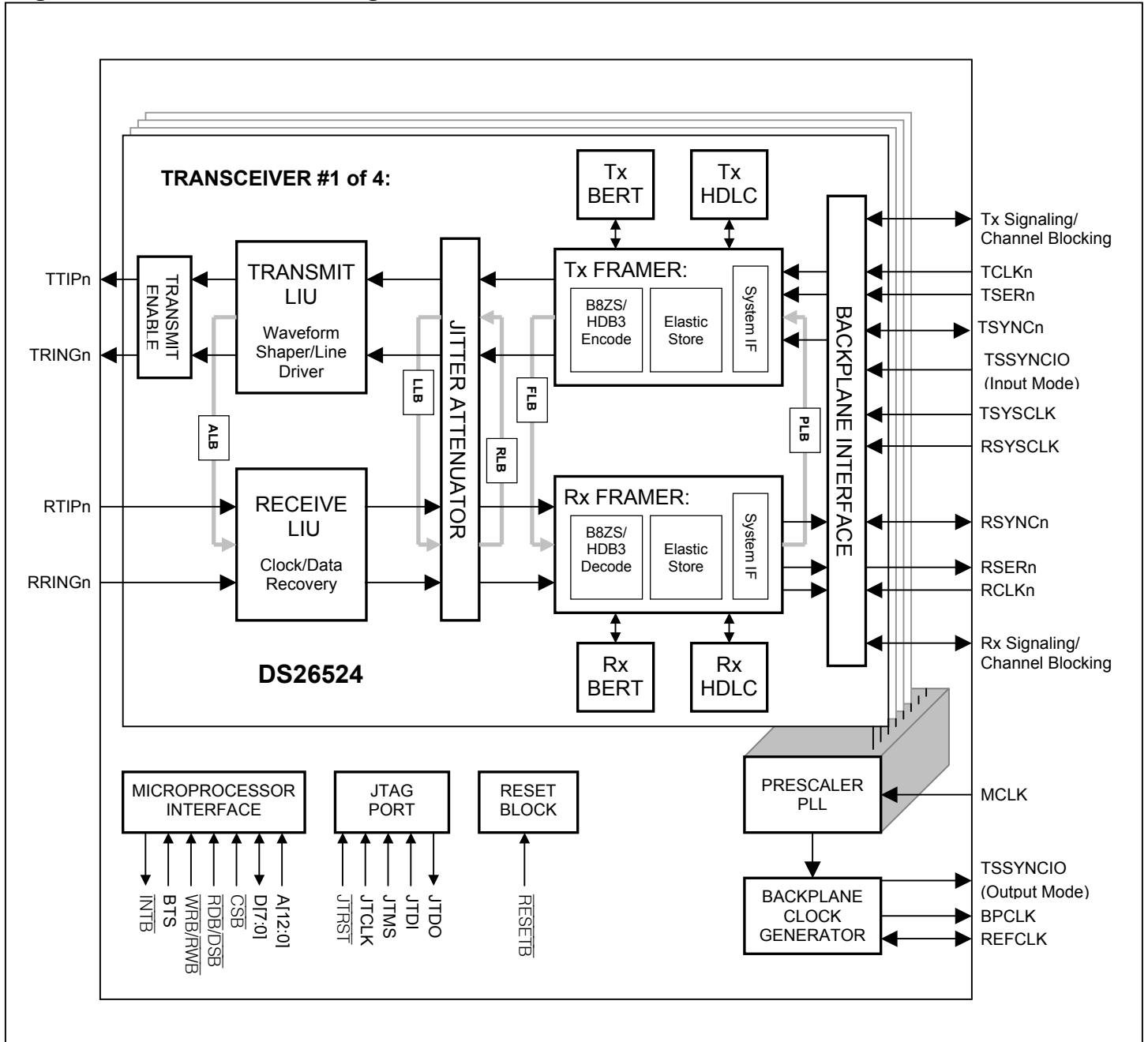


Figure 6-2. Detailed Block Diagram



7. PIN DESCRIPTIONS

7.1 Pin Functional Description

Table 7-1. Detailed Pin Descriptions

| NAME | PIN | TYPE | FUNCTION |
|------------------------|--------|-------------------------------|---|
| ANALOG TRANSMIT | | | |
| TTIP1 | A1, A2 | Analog Output, High Impedance | <p>Transmit Bipolar Tip for Transceiver 1 to 4. These pins are differential line driver tip outputs. These pins can be high impedance if:</p> <p>If TXENABLE is low, the TTIP/TRING will be high impedance. Note that if TXENABLE is low, the register settings for control of the TTIP/TRING are ignored and output is high impedance.</p> <p>The differential outputs of TTIP_n and TRING_n can provide internal matched impedance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω. The user has the option of turning off internal termination.</p> <p>Note: The two pins shown for each transmit bipolar tip (e.g., pins A1 and A2 for TTIP1) should be tied together.</p> |
| TTIP2 | H1, H2 | | |
| TTIP3 | J1, J2 | | |
| TTIP4 | T1, T2 | | |
| TRING1 | A3, B3 | Analog Output, High Impedance | <p>Transmit Bipolar Ring for Transceiver 1 to 4. These pins are differential line driver ring outputs. These pins can be high impedance if:</p> <p>If TXENABLE is low, the TTIP/TRING will be high impedance. Note that if TXENABLE is low, the register settings for control of the TTIP/TRING are ignored and output is high impedance.</p> <p>The differential outputs of TTIP_n and TRING_n can provide internal matched impedance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω. The user has the option of turning off internal termination.</p> <p>Note: The two pins shown for each transmit bipolar ring (e.g., pins A3 and B3 for TRING1) should be tied together.</p> |
| TRING2 | G3, H3 | | |
| TRING3 | J3, K3 | | |
| TRING4 | R3, T3 | | |
| TXENABLE | L13 | I | <p>Transmit Enable. If this pin is pulled low, all transmitter outputs (TTIP and TRING) are high impedance. The register settings for tri-state control of TTIP/TRING are ignored if TXENABLE is low. If TXENABLE is high, the particular driver can be tri-stated by the register settings.</p> |
| ANALOG RECEIVE | | | |
| RTIP1 | C1 | Analog Input | <p>Receive Bipolar Tip for Transceiver 1 to 4. The differential inputs of RTIP_n and RRING_n can provide internal matched impedance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω. The user has the option of turning off internal termination via the LIU Receive Impedance and Sensitivity Monitor register (LRISMR).</p> |
| RTIP2 | F1 | | |
| RTIP3 | L1 | | |
| RTIP4 | P1 | | |
| RRING1 | C2 | Analog Input | <p>Receive Bipolar Ring for Transceiver 1 to 4. The differential inputs of RTIP_n and RRING_n can provide internal matched impedance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω. The user has the option of turning off internal termination via the LIU Receive Impedance and Sensitivity Monitor register (LRISMR).</p> |
| RRING2 | F2 | | |
| RRING3 | L2 | | |
| RRING4 | P2 | | |
| TRANSMIT FRAMER | | | |
| TSER1 | F6 | I | <p>Transmit NRZ Serial Data. These pins are sampled on the falling edge of TCLK when the transmit-side elastic store is disabled. These pins are sampled on the falling edge of TSYCLK when the transmit-side elastic store is enabled.</p> <p>In IBO mode, data for multiple framers can be used in high-speed multiplexed scheme. This is described in Section 8.8.2. The table there presents the combination of framer data for each of the streams.</p> <p>TSYCLK is used as a reference when IBO is invoked.</p> |
| TSER2 | E7 | | |
| TSER3 | R4 | | |
| TSER4 | N7 | | |

| NAME | PIN | TYPE | FUNCTION |
|-----------------|-----|------|--|
| TCLK1 | C5 | | Transmit Clock. A 1.544MHz or a 2.048MHz primary clock. Used to clock data through the transmit side of the transceiver. TSER data is sampled on the falling edge of TCLK. TCLK is used to sample TSER when the elastic store is not enabled or IBO is not used. |
| TCLK2 | D7 | | |
| TCLK3 | P5 | | |
| TCLK4 | L8 | I | When the elastic store is enabled, TCLKn is used as the internal transmit clock for the framer side or the elastic store, including the transmit framer and LIU. With the elastic store enabled, TCLKn can be either synchronous or asynchronous to TSYCLKn, which either prevents or allows for slips. In addition, when IBO mode is enabled, TCLKn must be synchronous to TSYCLKn, which prevents slips in the elastic store. Note: This clock must be provided for proper device operation. The only exception is when the TCR3 register is configured to source TCLK internally from RCLK. |
| TSYSCLK | P13 | I | Transmit System Clock. 1.544MHz, 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz clock. Only used when the transmit-side elastic store function is enabled. Should be tied low in applications that do not use the transmit-side elastic store. This is a common clock that is used for the transmitters. The clock can be 4.096MHz, 8.912MHz, or 16.384MHz when IBO mode is used. |
| TSYNC1 | B4 | I/O | Transmit Synchronization. A pulse at these pins establishes either frame or multiframe boundaries for the transmit side. These signals can also be programmed to output either a frame or multiframe pulse. If these pins are set to output pulses at frame boundaries, they can also be set to output double-wide pulses at signaling frames in T1 mode. The operation of these signals is synchronous with TCLK. |
| TSYNC2 | F7 | | |
| TSYNC3 | M6 | | |
| TSYNC4 | M7 | | |
| TSSYNCIO | N13 | I/O | Transmit System Synchronization In. Only used when the transmit-side elastic store is enabled. A pulse at this pin establishes either frame or multiframe boundaries for the transmit side. Note that if the elastic store is enabled, frame or multiframe boundary will be established for all four transmitters. Should be tied low in applications that do not use the transmit-side elastic store. The operation of this signal is synchronous with TSYCLK. Transmit System Synchronization Out. If configured as an output, an 8kHz pulse synchronous to the BPCLK will be generated. This pulse in combination with BPCLK can be used as an IBO master. The BPCLK can be sourced to RSYCLK, TSYCLK, and TSSYNCIO as a source to RSYNC, and TSSYNCIO of DS26524 or RSYNC and TSSYNC of other Dallas Semiconductor parts. |
| TSIG1 | D5 | I | Transmit Signaling. When enabled, this input samples signaling bits for insertion into outgoing PCM data stream. Sampled on the falling edge of TCLK when the transmit-side elastic store is disabled. Sampled on the falling edge of TSYCLK when the transmit-side elastic store is enabled. In IBO mode, the TSIG streams can run up to 16.384MHz. |
| TSIG2 | A6 | | |
| TSIG3 | T4 | | |
| TSIG4 | R6 | | |
| TCHBLK/ CLK1 | A5 | O | Transmit Channel Block/Transmit Channel Block Clock. A dual function pin. TCHBLK is a user-programmable output that can be forced high or low during any of the channels. It is synchronous with TCLK when the transmit-side elastic store is disabled. It is synchronous with TSYCLK when the transmit-side elastic store is enabled. It is useful for blocking clocks to a serial UART or LAPD controller in applications where not all channels are used such as Fractional T1, Fractional E1, 384kbps (H0), 768kbps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning. TCHCLK. TCHCLKn is a dual function pin that can output either a gapped clock or a channel clock. In gapped clock mode, TCHCLKn is a N x 64kHz fractional clock that is software programmable for 0 to 24 channels and the F-bit (T1) or 0 to 32 channels (E1). In channel clock mode, TCHCLKn is a 192kHz (T1) or 256kHz (E1) clock that pulses high during the LSB of each channel. It is useful for parallel-to-serial conversion of channel data. In either mode, TCHCLKn is synchronous with TCLKn when the receive-side elastic store is disabled or it is synchronous with TSYCLKn when the receive-side elastic store is enabled. The mode of TCHCLKn is determined by the TGCLKEN bit in the TESCR register. |
| TCHBLK/ CLK2 | C7 | | |
| TCHBLK/ CLK3 | L7 | | |
| TCHBLK/ CLK4 | P7 | | |

| NAME | PIN | TYPE | FUNCTION |
|------------------------|-----|------|--|
| RECEIVE FRAMER | | | |
| RSER1 | E5 | O | Received Serial Data. Received NRZ serial data. Updated on rising edges of RCLK when the receive-side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive-side elastic store is enabled. When IBO mode is used, the RSER pins can output data for multiple framers. The RSER data is synchronous to RSYSCLK. This is described in Section 8.8.2 . |
| RSER2 | D6 | | |
| RSER3 | N4 | | |
| RSER4 | N6 | | |
| RCLK1 | F4 | O | Receive Clock. A 1.544MHz (T1) or 2.048MHz (E1) clock that is used to clock data through the receive-side framer. This clock is recovered from the signal at RTIP and RRING. RSER data is output on the rising edge of RCLK. RCLK is used to output RSER when the elastic store is not enabled or IBO is not used. When the elastic store is enabled or IBO is used, the RSER is clocked by RSYSCLK. |
| RCLK2 | G4 | | |
| RCLK3 | L4 | | |
| RCLK4 | M4 | | |
| RSYSCLK | L12 | I | Receive System Clock. 1.544MHz, 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz receive backplane clock. Only used when the receive-side elastic store function is enabled. Should be tied low in applications that do not use the receive-side elastic store. Multiple of 2.048MHz is expected when the IBO mode is used. Note that RSYSCLK is used for all four transceivers. |
| RSYNC1 | A4 | I/O | Receive Synchronization. If the receive-side elastic store is enabled, then this signal is used to input a frame or multiframe boundary pulse. If set to output frame boundaries, then RSYNC can be programmed to output double-wide pulses on signaling frames in T1 mode. In E1 mode, RSYNC out can be used to indicate CAS and CRC-4 multiframe. The DS26524 can accept H.100-compatible synchronization signal. The default direction of this pin at power-up is input, as determined by the RSIO control bit in the RIOCR.2 register. |
| RSYNC2 | B6 | | |
| RSYNC3 | N5 | | |
| RSYNC4 | T6 | | |
| RMSYNC1/ RFSYNC1 | C4 | O | Receive Multiframe/Frame Synchronization. A dual function pin to indicate frame or multiframe synchronization. RFSYNC is an extracted 8kHz pulse, one RCLK wide that identifies frame boundaries. RMSYNC is an extracted pulse, one RCLK wide (elastic store disabled) or one RSYSCLK wide (elastic store enabled), that identifies multiframe boundaries. When the receive elastic store is enabled, the RMSYNC signal indicates the multiframe sync on the system (backplane) side of the elastic store. In E1 mode, this pin can indicate either the CRC-4 or CAS multiframe as determined by the RSMS2 control bit in the Receive I/O Configuration register (RIOCR.1). |
| RMSYNC2/ RFSYNC2 | C6 | | |
| RMSYNC3/ RFSYNC3 | P4 | | |
| RMSYNC4/ RFSYNC4 | P6 | | |
| RSIG1 | D4 | O | Receive Signaling. Outputs signaling bits in a PCM format. Updated on rising edges of RCLK when the receive-side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive-side elastic store is enabled. |
| RSIG2 | E6 | | |
| RSIG3 | M5 | | |
| RSIG4 | R5 | | |
| AL/ RSIGF/ FLOS1 | C3 | O | Analog Loss/Receive-Signaling Freeze/Framer LOS. Analog LOS reflects the LOS (loss of signal) detected by the LIU front-end and framer LOS is LOS detection by the corresponding framer; the same pins can reflect receive-signaling freeze indications. This selection can be made by settings in the Global Transceiver Clock Control register (GTCCR). If framer LOS is selected, this pin can be programmed to toggle high when the framer detects an LOS condition, or when the signaling data is frozen via either automatic or manual intervention. The indication is used to alert downstream equipment of the condition. |
| AL/ RSIGF/ FLOS2 | F3 | | |
| AL/ RSIGF/ FLOS3 | L3 | | |
| AL/ RSIGF/ FLOS4 | P3 | | |
| RLF/ LTC1 | D3 | O | Receive Loss of Frame/Loss of Transmit Clock. This pin can be programmed to either toggle high when the synchronizer is searching for the frame and multiframe, or to toggle high if the TCLK pin has not been toggled for approximately three clock periods. |
| RLF/ LTC2 | E3 | | |
| RLF/ LTC3 | M3 | | |
| RLF/ LTC4 | N3 | | |

| NAME | PIN | TYPE | FUNCTION |
|---------------------------------|-----|------|---|
| RCHBLK/ CLK1 | E4 | O | <p>Receive Channel Block/Receive Channel Block Clock. This pin can be configured to output either RCHBLK or RCHCLK. RCHBLK is a user-programmable output that can be forced high or low during any of the 24 T1 or 32 E1 channels. It is synchronous with RCLK when the receive-side elastic store is disabled. It is synchronous with RSYSCLK when the receive-side elastic store is enabled. This pin is useful for blocking clocks to a serial UART or LAPD controller in applications where not all channels are used such as fractional service, 384kbps service, 768kbps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning.</p> <p>RCHCLK. RCHCLKn is a dual function pin that can output either a gapped clock or a channel clock. In gapped clock mode, RCHCLKn is a N x 64kHz fractional clock that is software programmable for 0 to 24 channels and the F-bit (T1) or 0 to 32 channels (E1). In channel clock mode, RCHCLKn is a 192kHz (T1) or 256kHz (E1) clock that pulses high during the LSB of each channel. It is useful for parallel-to-serial conversion of channel data. In either mode, RCHCLK is synchronous with RCLKn when the receive-side elastic store is disabled or it is synchronous with RSYSCLKn when the receive-side elastic store is enabled. The mode of RCHCLKn is determined by the RGCLKEN bit in the RESCR register.</p> |
| RCHBLK/ CLK2 | B5 | | |
| RCHBLK/ CLK3 | L6 | | |
| RCHBLK/ CLK4 | T5 | | |
| BPCLK | E8 | O | <p>Backplane Clock. Programmable clock output that can be set to 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz. The reference for this clock can be RCLK from any of the LIU, 1.544MHz, or 2.048MHz frequency derived from MCLK or an external reference clock. This allows for the IBO clock to reference from external source or T1J1E1 recovered clock or the MCLK oscillator.</p> |
| MICROPROCESSOR INTERFACE | | | |
| A12 | C8 | I | <p>Address [12:0]. This bus selects a specific register in the DS26524 during read/write access. A12 is the MSB and A0 is the LSB.</p> |
| A11 | A8 | | |
| A10 | B8 | | |
| A9 | F8 | | |
| A8 | B9 | | |
| A7 | A9 | | |
| A6 | C9 | | |
| A5 | D9 | | |
| A4 | E9 | | |
| A3 | F9 | | |
| A2 | B10 | | |
| A1 | A10 | | |
| A0 | C10 | | |
| D7 | T9 | I | <p>Data [7:0]. This 8-bit, bidirectional data bus is used for read/write access of the DS26524 information and control registers. D7 is the MSB and D0 is the LSB.</p> |
| D6 | N9 | | |
| D5 | M9 | | |
| D4 | R8 | | |
| D3 | T8 | | |
| D2 | P8 | | |
| D1 | L9 | | |
| D0 | N8 | | |
| $\overline{\text{CSB}}$ | T7 | I | <p>Chip-Select Bar. This active-low signal is used to qualify register read/write accesses. The $\overline{\text{RDB/DSB}}$ and $\overline{\text{WRB}}$ signals are qualified with $\overline{\text{CSB}}$.</p> |
| $\overline{\text{RDB/DSB}}$ | M8 | I | <p>Read-Data Bar/Data-Strobe Bar. This active-low signal along with $\overline{\text{CSB}}$ qualifies read access to one of the DS26524 registers. The DS26524 drives the data bus with the contents of the addressed register while $\overline{\text{RDB}}$ and $\overline{\text{CSB}}$ are low.</p> |
| $\overline{\text{WRB/RWB}}$ | R7 | I | <p>Write-Read Bar/Read-Write Bar. This active-low signal along with $\overline{\text{CSB}}$ qualifies write access to one of the DS26524 registers. Data at D[7:0] is written into the addressed register at the rising edge of $\overline{\text{WRB}}$ while $\overline{\text{CSB}}$ is low.</p> |

| NAME | PIN | TYPE | FUNCTION |
|----------------------------|-----|-------------------|--|
| $\overline{\text{INTB}}$ | R9 | U | Interrupt Bar. This active-low, open-drain output is asserted when an unmasked interrupt event is detected. $\overline{\text{INTB}}$ will be deasserted when all interrupts have been acknowledged and serviced. Extensive mask bits are provided at the global level, framer, LIU, and BERT level. |
| BTS | M13 | I | Bus Type Select. Set high to select Motorola bus timing, low to select Intel bus timing. This pin controls the function of the RDB/DSB and WRB pins. |
| SYSTEM INTERFACE | | | |
| MCLK | B7 | I | Master Clock. This is an independent free-running clock whose input can be a multiple of 2.048MHz \pm 50ppm or 1.544MHz \pm 50ppm. The clock selection is available by bits MPS0 and MPS1 and FREQSEL. Multiple of 2.048MHz can be internally adapted to 1.544MHz. Multiple of 1.544MHz can be adapted to 2.048MHz. Note that TCLK must be 2.048MHz for E1 and 1.544MHz for T1/J1 operation. See Table 9-12 . |
| $\overline{\text{RESETB}}$ | J12 | I | Reset Bar. Active-low reset. This input forces the complete DS26524 reset. This includes reset of the registers, framers, and LIUs. |
| REFCLKIO | A7 | I/O | Reference Clock Input/Output <i>Input:</i> A 2.048MHz or 1.544MHz clock input. This clock can be used to generate the backplane clock. This allows for the users to synchronize the system backplane with the reference clock. The other options for the backplane clock reference are LIU-received clocks or MCLK. <i>Output:</i> This signal can also be used to output a 1.544MHz or 2.048MHz reference clock. This allows for multiple DS26524s to share the same reference for generation of the backplane clock. Hence, in a system consisting of multiple DS26524s, one can be a master and others a slave using the same reference clock. |
| TEST | | | |
| DIGIOEN | D8 | I, Pullup | Digital Enable. When this pin and $\overline{\text{JTRST}}$ are pulled low, all digital I/O pins are placed in a high-impedance state. If this pin is high the digital I/O pins operate normally. This pin must be connected to V_{DD} for normal operation. |
| $\overline{\text{JTRST}}$ | L5 | I, Pullup | JTAG Reset. $\overline{\text{JTRST}}$ is used to asynchronously reset the test access port controller. After power-up, $\overline{\text{JTRST}}$ must be toggled from low to high. This action sets the device into the JTAG DEVICE ID mode. Pulling $\overline{\text{JTRST}}$ low restores normal device operation. $\overline{\text{JTRST}}$ is pulled high internally via a 10k Ω resistor operation. If boundary scan is not used, this pin should be held low. |
| JTMS | K4 | I, Pullup | JTAG Mode Select. This pin is sampled on the rising edge of JTCLK and is used to place the test access port into the various defined IEEE 1149.1 states. This pin has a 10k Ω pullup resistor. |
| JTCLK | F5 | I | JTAG Clock. This signal is used to shift data into JTDI on the rising edge and out of JTDO on the falling edge. |
| JTDI | H4 | I, Pullup | JTAG Data In. Test instructions and data are clocked into this pin on the rising edge of JTCLK. This pin has a 10k Ω pullup resistor. |
| JTDO | J4 | O, High impedance | JTAG Data Out. Test instructions and data are clocked out of this pin on the falling edge of JTCLK. If not used, this pin should be left unconnected. |

| NAME | PIN | TYPE | FUNCTION |
|-----------------------|---------------------|------|---|
| POWER SUPPLIES | | | |
| ATVDD1 | B1 | — | 3.3V Analog Transmit Power Supply. These V_{DD} inputs are used for the transmit LIU sections of the DS26524. |
| ATVDD2 | G1 | | |
| ATVDD3 | K1 | | |
| ATVDD4 | R1 | | |
| ATVDD5 | R16 | | |
| ATVDD6 | K16 | | |
| ATVDD7 | G16 | | |
| ATVDD8 | B16 | | |
| ATVSS1 | B2 | — | Analog Transmit V_{SS}. These pins are used for transmit analog V_{SS} . |
| ATVSS2 | G2 | | |
| ATVSS3 | K2 | | |
| ATVSS4 | R2 | | |
| ATVSS5 | R15 | | |
| ATVSS6 | K15 | | |
| ATVSS7 | G15 | | |
| ATVSS8 | B15 | | |
| ARVDD1 | D1 | — | 3.3V Analog Receive Power Supply. These V_{DD} inputs are used for the receive LIU sections of the DS26524. |
| ARVDD2 | E1 | | |
| ARVDD3 | M1 | | |
| ARVDD4 | N1 | | |
| ARVDD5 | N16 | | |
| ARVDD6 | M16 | | |
| ARVDD7 | E16 | | |
| ARVDD8 | D16 | | |
| ARVSS1 | D2 | — | Analog Receive V_{SS}. These pins are used for analog V_{SS} for the receivers. |
| ARVSS2 | E2 | | |
| ARVSS3 | M2 | | |
| ARVSS4 | N2 | | |
| ARVSS5 | N15 | | |
| ARVSS6 | M15 | | |
| ARVSS7 | E15 | | |
| ARVSS8 | D15 | | |
| ACVDD | H7 | — | Analog Clock Conversion V_{DD}. This V_{DD} input is used for the clock conversion unit of the DS26524. |
| ACVSS | J7 | — | Analog Clock V_{SS}. This pin is used for clock converter analog V_{SS} . |
| DVDD | G5–G12, H8, H9 | — | 3.3V Power Supply for Digital Framers |
| DVDDIO | H5, H6, H10, H11 | — | 3.3V Power Supply for I/Os |

| NAME | PIN | TYPE | FUNCTION |
|--------|--|------|--|
| DVSS | A11, A13, B11, B13, C11, C13, D12, D13, E10, F10, H12, H13, J8, J9, K5–K12, L10, L11, M10, N10, N11, P12, R10, R12, T10, T12 | — | Digital Ground for the Framers |
| DVSSIO | J5, J6, J10, J11 | — | Digital Ground for the I/Os |
| N.C. | A12, A14, A15, A16, B12, B14, C12, C14, C15, C16, D10, D11, D14, E11–E14, F11–F16, G13, G14, H14, H15, H16, J13–J16, K13, K14, L14, L15, L16, M11, M12, M14, N12, N14, P9, P10, P11, P14, P15, P16, R11, R13, R14, T11, T13–T16 | — | No Connection. These pins must not be connected to V_{DD} or V_{SS} . |

8. FUNCTIONAL DESCRIPTION

8.1 Processor Interface

Microprocessor control of the DS26524 is accomplished through the 28 hardware pins of the microprocessor port. The 8-bit parallel data bus can be configured for Intel or Motorola modes of operation with the bus type select (BTS) pin. When the BTS pin is a logic 0, bus timing is in Intel mode, as shown in [Figure 12-1](#) and [Figure 12-2](#). When the BTS pin is a logic 1, bus timing is in Motorola mode, as shown in [Figure 12-3](#) and [Figure 12-4](#). The address space is mapped through the use of 13 address lines, A[12:0]. Multiplexed mode is not supported on the processor interface.

The chip-select bar ($\overline{\text{CSB}}$) pin must be brought to a logic-low level to gain read and write access to the microprocessor port. With Intel timing selected, the read-data bar ($\overline{\text{RDB}}$) and write-read bar ($\overline{\text{WRB}}$) pins are used to indicate read and write operations and latch data through the interface. With Motorola timing selected, the read-write bar ($\overline{\text{RWB}}$) pin is used to indicate read and write operations while the data-strobe bar ($\overline{\text{DSB}}$) pin is used to latch data through the interface.

The interrupt output pin ($\overline{\text{INTB}}$) is an open-drain output that asserts a logic-low level upon a number of software maskable interrupt conditions. This pin is normally connected to the microprocessor interrupt input. The device has a bulk write mode that allows a microprocessor to write all four internal transceivers with each bus write cycle. By setting the BWE bit ([GTCR1.2](#)), each port write cycle will write to all four framers, LIUs, or BERTs at the same time. The BWE bit must be cleared before normal write operation is resumed. This function is useful for device initialization. The register map is shown in [Figure 9-1](#).

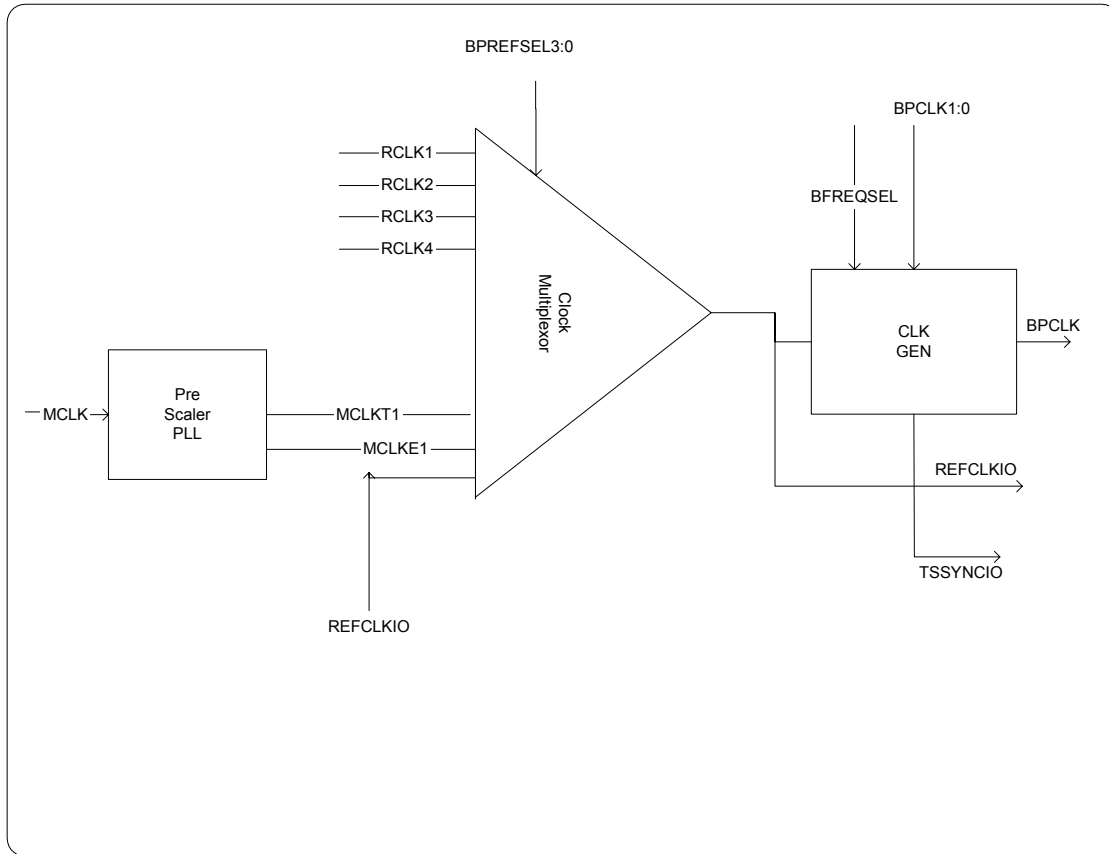
8.2 Clock Structure

The user should provide a system clock to the MCLK input of 2.048MHz, 1.544MHz, or a multiple of up to 8x the T1 and E1 frequencies. To meet many specifications, the MCLK source should have ± 50 ppm accuracy.

8.2.1 Backplane Clock Generation

The DS26524 provides facility for provision of BPCLK at 2.048MHz, 4.096MHz, 8.192MHz, 16.384MHz (see [Figure 8-1](#)). The Global Transceiver Clock Control register ([GTCCR](#)) is used to control the backplane clock generation. This register is also used to program REFCLKIO as an input or output. REFCLKIO can output MCLKT1 or MCLKE1 as shown in [Figure 8-1](#).

This backplane clock and frame pulse (TSSYNCIO) can be used by the DS26524 and other IBO-equipped devices as an IBO bus master. Hence, the DS26524 provides the 8kHz sync pulse and 4MHz, 8MHz, and 16MHz clock. This can be used by the link layer devices and frames connected to the IBO bus.

Figure 8-1. Backplane Clock Generation

The reference clock for the backplane clock generator can be as follows:

- External Master Clock. A prescaler can be used to generate T1 or E1 frequency.
- External Reference Clock REFCLKIO. This allows for multiple DS26524s to use the backplane clock from a common reference.
- Internal LIU recovered RCLKs 1 to 4.
- The clock generator can be used to generate BPCLK of 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz for the IBO.
- If MCLK or RCLK are used as a reference, REFCLKIO can be used to provide a 2.048MHz or 1.544MHz clock for external use.

8.3 Resets and Power-Down Modes

A hardware reset is issued by forcing the $\overline{\text{RESETB}}$ pin to logic-low. The $\overline{\text{RESETB}}$ input pin resets all framers, LIUs, and BERTs. Note that not all registers are cleared to 00h on a reset condition. **The register space must be reinitialized to appropriate values after a hardware or software reset has occurred.** This includes writing reserved locations to 00h.

The DS26524 has several features included to reduce power consumption. The LIU transmitters can be powered down by setting the TPDE bit in the LIU Maintenance Control register ([LMCR](#)). Note that powering down the transmit LIU results in a high-impedance state for the corresponding TTIP and TRING pins and reduced operating current. The RPDE bit in the [LMCR](#) register can be used to power down the LIU receiver.

The TE (transmit enable) bit in the [LMCR](#) register can be used to disable the TTIP and TRING outputs and place them in a high-impedance mode, while keeping the LIU in an active state (powered up). This is useful for equipment protection-switching applications.

Table 8-1. Reset Functions

| RESET FUNCTION | LOCATION | COMMENTS |
|---------------------------------|--|---|
| Hardware Device Reset | $\overline{\text{RESETB}}$ | Transition to a logic 0 level resets the DS26524. |
| Hardware JTAG Reset | $\overline{\text{JTRST}}$ | Resets the JTAG test port. |
| Global Framer and BERT Reset | GFSRR .0:3 | Writing to these bits resets the framer and BERT (transmit and receive). |
| Global LIU Reset | GLSRR .0:3 | Writing to these bits resets the associated LIU. |
| Framer Receive Reset | RMMR .1 | Writing to this bit resets the receive framer. |
| Framer Transmit Reset | TMMR .1 | Writing to this bit resets the transmit framer. |
| HDLC Receive Reset | RHC .6 | Writing to this bit resets the receive HDLC controller. |
| HDLC Transmit Reset | THC 1.5 | Writing to this bit resets the transmit HDLC controller. |
| Elastic Store Receive Reset | RESRCR .2 | Writing to this bit resets the receive elastic store. |
| Elastic Store Transmit Reset | TESRCR .2 | Writing to this bit resets the transmit elastic store. |
| Bit Oriented Code Receive Reset | T1RBOCC .7 | Writing to this bit resets the receive BOC controller. |
| Loop Code Integration Reset | T1RDNCD1 , T1RUPCD1 | Writing to these registers resets the programmable in-band code integration period. |
| Spare Code Integration Reset | T1RSCD1 | Writing to this register resets the programmable in-band code integration period. |

8.4 Initialization and Configuration

8.4.1 Example Device Initialization Sequence

STEP 1: Reset the device by pulling the $\overline{\text{RESETB}}$ pin low, applying power to the device, or by using the software reset bits outlined in Section 8.3. Clear all reset bits. Allow time for the reset recovery.

STEP 2: Check the device ID in the Device Identification register ([IDR](#)).

STEP 3: Write the [GTCCR](#) register to correctly configure the system clocks. If supplying a 1.544MHz MCLK, follow this write with at least a 300ns delay to allow the clock system to properly adjust.

STEP 4: Write the entire remainder of the register space for each port with 00h, including reserved register locations.

STEP 5: Choose T1/J1 or E1 operation for the framers by configuring the T1/E1 bit in the [TMMR](#) and [RMMR](#) registers for each framer. Set the FRM_EN bit to 1 in the [TMMR](#) and [RMMR](#) registers. If using software transmit signaling in E1 mode, program the [E1TAF](#) and [E1TNAF](#) registers as required. Configure the framer Transmit Control registers ([TCR1:TCR4](#)). Configure the Framer Receive Control registers ([RCR1](#) (T1)/[RCR1](#) (E1), [T1RCR2/E1RCR2](#), [RCR3](#)). Configure other framer features as appropriate.

STEP 6: Choose T1/J1 or E1 operation for the LIUs by configuring the T1J1E1S bit in the [LTRCR](#) register. Configure the line build-out for each LIU. Configure other LIU features as appropriate. Set the TE bit to turn on the TTIP and TRING outputs.

STEP 7: Configure the elastic stores, HDLC controller, and BERT as needed.

STEP 8: Set the INIT_DONE bit in the [TMMR](#) and [RMMR](#) registers for each framer.

8.5 Global Resources

All four framers share a common microprocessor port. All ports share a common MCLK, and there is a common software-configurable BPCLK output. A set of global registers are located at 0F0h–0FFh and include global resets, global interrupt status, interrupt masking, clock configuration, and the device ID registers. See the global register definitions in [Table 9-2](#). A common JTAG controller is used.

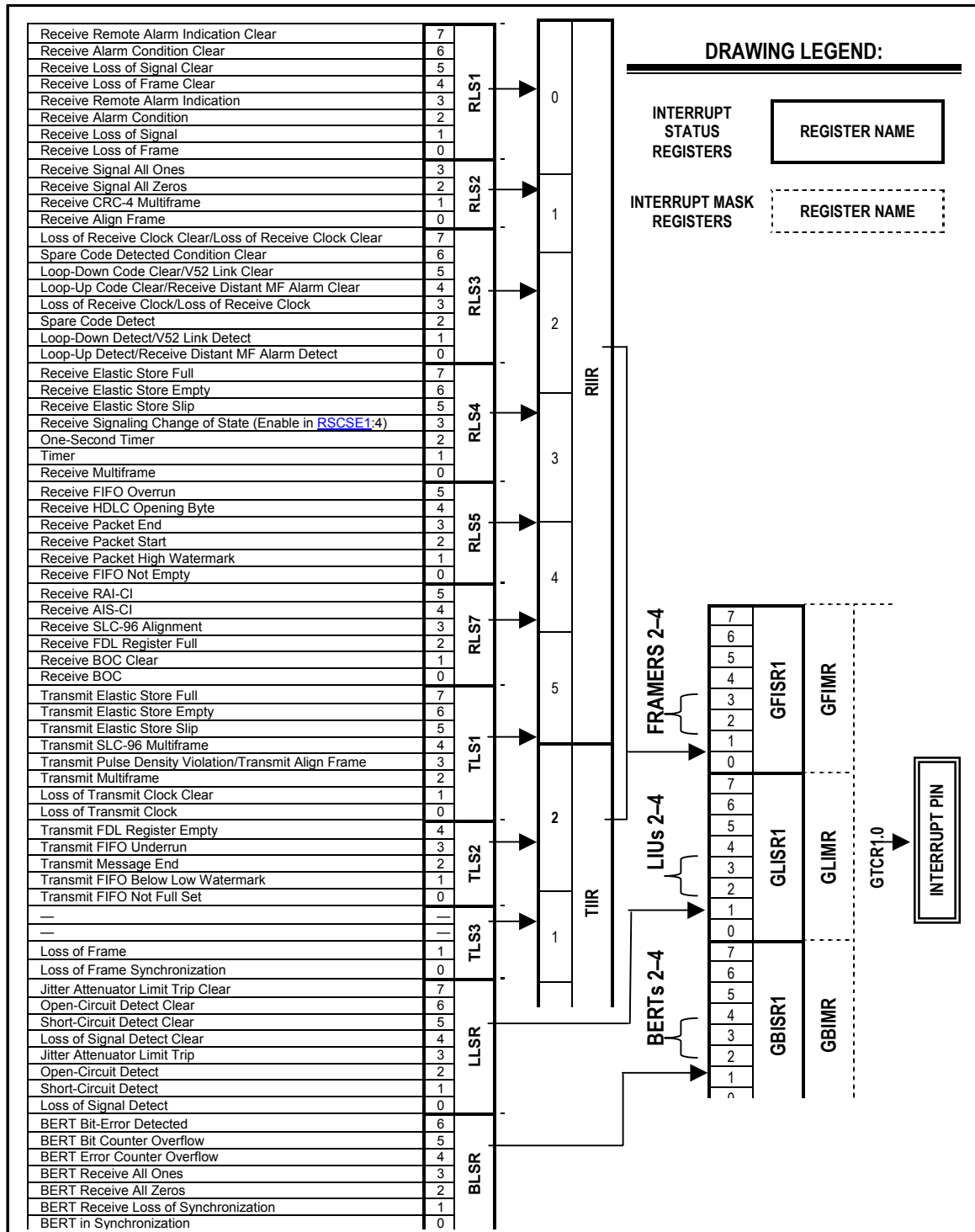
8.6 Per-Port Resources

Each port has an associated framer, LIU, BERT, jitter attenuator, and transmit/receive HDLC controller. Each of the per-port functions has its own register space.

8.7 Device Interrupts

[Figure 8-2](#) diagrams the flow of interrupt conditions from their source status bits through the multiple levels of information registers and mask bits to the interrupt pin. When an interrupt occurs, the host can read the global interrupt information registers [GFISR](#), [GLISR](#), and [GBISR](#) to identify which of the four transceivers is causing the interrupt(s). The host can then read the specific transceiver's interrupt information registers ([TIIR](#), [RIIR](#)) and the latched status registers ([LLSR](#), [BLSR](#)) to further identify the source of the interrupt(s). If [TIIR](#) or [RIIR](#) is the source, the host will then read the transmit-latched status or the receive-latched status registers for the source of the interrupt. All interrupt information register bits are real-time bits that clear once the appropriate interrupt has been serviced and cleared, as long as no additional, unmasked interrupt condition is present in the associated status register. The host must clear all latched status bits by writing a 1 to the bit location of the interrupt condition that has been serviced. Latched status bits that have been masked by the interrupt mask registers are masked from the interrupt information registers. The interrupt mask register bits prevent individual latched status conditions from generating an interrupt, but they do not prevent the latched status bits from being set. Therefore, when servicing interrupts, the user should XOR the latched status with the associated interrupt mask in order to exclude bits for which the user wished to prevent interrupt service. This architecture allows the application host to periodically poll the latched status bits for noninterrupt conditions, while using only one set of registers.

Figure 8-2. Device Interrupt Information Flow Diagram



8.8 System Backplane Interface

The DS26524 provides a versatile backplane interface that can be configured to the following:

- Transmit and receive two-frame elastic stores
- Mapping of T1 channels into a 2.048MHz backplane
- IBO mode for multiple framers to share the backplane signals
- Transmit and receive channel-blocking capability
- Fractional T1/E1/J1 support
- Hardware-based (through the backplane interface) or processor-based signaling
- Flexible backplane clock providing frequencies of 2.048MHz, 4.096MHz, 8.192MHz, 16.384MHz
- Backplane clock and frame pulse (TSSYNClOn) generator

8.8.1 Elastic Stores

The DS26524 contains dual two-frame elastic stores for each framer: one for the receive direction and one for the transmit direction. Both elastic stores are fully independent. The transmit- and receive-side elastic stores can be enabled/disabled independently of each other. Also, the transmit or receive elastic store can interface to either a 1.544MHz or 2.048/4.096/8.192/16.384MHz backplane without regard to the backplane rate for the other elastic store. Since the DS26524 has a common TSYCLK and RSYCLK for all four ports, the backplane signals in each direction must be synchronous for all ports on which the elastic stores are enabled. However, the transmit and receive signals are not required to be synchronous to each other. The TIOCR and RIOCR settings should be identical for all ports on which the elastic stores are enabled.

The elastic stores have two main purposes. First, they can be used for rate conversion. When the DS26524 is in the T1 mode, the elastic stores can rate convert the T1 data stream to a 2.048MHz backplane. In E1 mode the elastic store can rate convert the E1 data stream to a 1.544MHz backplane. Second, the elastic stores can be used to absorb the differences in frequency and phase between the T1 or E1 data stream and an asynchronous (i.e., not locked) backplane clock, which can be 1.544MHz or 2.048MHz. In this mode, the elastic stores manage the rate difference and perform controlled slips, deleting or repeating frames of data to manage the difference between the network and the backplane.

If the elastic store is enabled while in E1 mode, then either CAS or CRC-4 multiframe boundaries are indicated via the RMSYNC output as controlled by the RSMS2 control bit ([RIOCR.1](#)). If the user selects to apply a 1.544MHz clock to the RSYCLK pin, then the Receive Blank Channel Select registers ([RBCS1:RBCS4](#)) registers determine which channels of the received E1 data stream will be deleted. In this mode an F-bit location is inserted into the RSER data and set to 1. Also, in 1.544MHz applications, the RCHBLK output will not be active in Channels 25 to 32 (or in other words, RCBR4 is not active). If the two-frame elastic buffer either fills or empties, a controlled slip occurs. If the buffer empties, a full frame of data is repeated at RSER and the [RLS4.5](#) and [RLS4.6](#) bits are set to 1. If the buffer fills, a full frame of data is deleted and the [RLS4.5](#) and [RLS4.7](#) bits are set to 1.

The elastic stores can also be used to multiplex T1 or E1 data streams into higher backplane rates. This is the Interleave Bus Option (IBO), which is discussed in Section [8.8.2](#). [Table 8-2](#) shows the registers related to the elastic stores.

Table 8-2. Registers Related to the Elastic Store

| REGISTER | FRAMER ADDRESSES | FUNCTION |
|---|------------------|--|
| Receive I/O Configuration Register (RIOCR) | 084h | Sync and clock selection for the receiver. |
| Receive Elastic Store Control Register (RESCR) | 085h | Receive elastic store control. |
| Receive Latched Status Register 4 (RLS4) | 093h | Receive elastic store empty full status. |
| Receive Interrupt Mask Register 4 (RIM4) | 0A3h | Receive interrupt mask for elastic store. |
| Transmit Elastic Store Control Register (TESCR) | 185h | Transmit elastic control such as minimum mode. |
| Transmit Latched Status Register 1 (TLS1) | 190h | Transmit elastic store latched status. |
| Transmit Interrupt Mask Register 1 (TIM1) | 1A0h | Transmit elastic store interrupt mask. |

Note: The addresses shown are for Framer 1. Addresses for Framers 2 to 4 can be calculated using the following: Framer n = (Framer 1 address + $(n - 1) \times 200h$), where n = 2 to 4 for Framers 2 to 4.

8.8.1.1 Elastic Stores Initialization

There are two elastic store initializations that can be used to improve performance in certain applications: elastic store reset and elastic store align. Both of these involve the manipulation of the elastic store's read and write pointers and are useful primarily in synchronous applications (RSYSCLK/TSYSCLK are locked to RCLK/TCLK, respectively). The elastic store reset is used to minimize the delay through the elastic store. The elastic store align bit is used to "center" the read/write pointers to the extent possible.

Table 8-3. Elastic Store Delay After Initialization

| INITIALIZATION | REGISTER BIT | DELAY |
|------------------------------|-------------------------|--|
| Receive Elastic Store Reset | RESCR.2 | $N \text{ bytes} < \text{Delay} < 1 \text{ Frame} + N \text{ bytes}$ |
| Transmit Elastic Store Reset | TESCR.2 | $N \text{ bytes} < \text{Delay} < 1 \text{ Frame} + N \text{ bytes}$ |
| Receive Elastic Store Align | RESCR.3 | $1/2 \text{ Frame} < \text{Delay} < 1 \text{ } 1/2 \text{ Frames}$ |
| Transmit Elastic Store Align | TESCR.3 | $1/2 \text{ Frame} < \text{Delay} < 1 \text{ } 1/2 \text{ Frames}$ |

$N = 9$ for $RSZS = 0$; $N = 2$ for $RSZS = 1$.

8.8.1.2 Minimum Delay Mode

Elastic store minimum-delay mode can be used when the elastic store's system clock is locked to its network clock (i.e., RCLK locked to RSYSCLK for the receive side and TCLK locked to TSYSCLK for the transmit side). [RESCR.1](#) enables the receive elastic store minimum-delay mode. When enabled, the elastic stores are forced to a maximum depth of 32 bits instead of the normal two-frame depth. This feature is useful primarily in applications that interface to a 2.048MHz bus. Certain restrictions apply when minimum-delay mode is used. In addition to the restriction mentioned above, RSYNC must be configured as an output when the receive elastic store is in minimum-delay mode and TSYNC must be configured as an output when transmit minimum-delay mode is enabled. In this mode the SYNC outputs are always in frame mode (multiframe outputs are not allowed). In a typical application, RSYSCLK and TSYSCLK are locked to RCLK and RSYNC (frame-output mode) is connected to TSSYNCIO (frame-input mode). The slip zone select bit (RSZS at [RESCR.4](#)) must be set to 1. All the slip contention logic in the framer is disabled (since slips cannot occur). On power-up, after the RSYSCLK and TSYSCLK signals have locked to their respective network clock signals, the elastic store reset bit ([RESCR.2](#)) should be toggled from a 0 to 1 to ensure proper operation

8.8.1.3 Additional Receive Elastic Store Information

If the receive-side elastic store is enabled, the user must provide either a 1.544MHz or 2.048MHz clock at the RSYSCLK pin. See Section [8.8.2](#) for higher rate system-clock applications. The user has the option of either providing a frame/multiframe sync at the RSYNC pin or having the RSYNC pin provide a pulse on frame/multiframe boundaries. If signaling reinsertion is enabled, the robbed-bit signaling data is realigned to the multiframe sync input on RSYNC. Otherwise, a multiframe sync input on RSYNC is treated as a simple frame boundary by the elastic store. The framer always indicates frame boundaries on the network side of the elastic store via the RFSYNC output, whether the elastic store is enabled or not. Multiframe boundaries are always indicated via the RMSYNC output. If the elastic store is enabled, RMSYNC outputs the multiframe boundary on the backplane side of the elastic store. When the device is receiving T1 and the backplane is enabled for 2.048MHz operation, the RMSYNC signal outputs the T1 multiframe boundaries as delayed through the elastic store. When the device is receiving E1 and the backplane is enabled for 1.544MHz operation, the RMSYNC signal outputs the E1 multiframe boundaries as delayed through the elastic store.

If the user selects to apply a 2.048MHz clock to the RSYSCLK pin, the user can use the Receive Blank Channel Select registers ([RBCS1:RBCS4](#)) to determine which channels will have the data output at RSER forced to all ones.

8.8.1.4 Receiving Mapped T1 Channels from a 2.048MHz Backplane

Setting the TSCLKM bit ([TIOCR.4](#)) enables the transmit elastic store to operate with a 2.048MHz backplane (32 time slots/frame). In this mode the user can choose which of the backplane channels on TSER will be mapped into the T1 data stream by programming the Transmit Blank Channel Select registers ([TBCS1:TBCS4](#)). A logic 1 in the associated bit location forces the transmit elastic store to ignore backplane data for that channel. Typically the user will want to program eight channels to be ignored. The default (power-up) configuration ignores channels 25 to 32, so that the first 24 backplane channels are mapped into the T1 transmit data stream.

For example, if the user desired to transmit data from the 2.048MHz backplane channels 2 to 16 and 18 to 26, the [TBCS1:TBCS4](#) registers should be programmed as follows:

```
TBCS1 = 01h  :: ignore backplane channel 1 ::
TBCS2 = 00h
TBCS3 = 01h  :: ignore backplane channel 17 ::
TBCS4 = FCh  :: ignore backplane channels 27 to 32 ::
```

8.8.1.5 Mapping T1 Channels onto a 2.048MHz Backplane

Setting the RSCLKM bit ([RIOCR.4](#)) enables the receive elastic store to operate with a 2.048MHz backplane (32 time slots/frame). In this mode the user can choose which of the backplane channels on RSER receive the T1 data by programming the Receive Blank Channel Select registers ([RBCS1:RBCS4](#)). A logic 1 in the associated bit location forces RSER high for that backplane channel. Typically the user will want to program eight channels to be blanked. The default (power-up) configuration blanks channels 25 to 32, so that the 24 T1 channels are mapped into the first 24 channels of the 2.048MHz backplane. If the user chooses to blank channel 1 (TS0) by setting [RBCS1.0](#) = 1, the F-bit will be passed into the MSB of TS0 on RSER.

For example, if:

```
RBCS1 = 01h
RBCS2 = 00h
RBCS3 = 01h
RBCS4 = FCh
```

Then on RSER:

```
Channel 1 (MSB) = F-bit
Channel 1 (bits 1 to 7) = all ones
Channels 2 to 16 = T1 channels 1 to 15
Channel 17 = all ones
Channels 18 to 26 = T1 channels 16 to 24
Channels 27 to 32 = all ones
```

Note that when two or more sequential channels are chosen to be blanked, the receive slip zone select bit should be set to 0. If the blank channels are distributed (such as 1, 5, 9, 13, 17, 21, 25, 29), the RSZS bit can be set to 1, which can provide a lower occurrence of slips in certain applications.

If the two-frame elastic buffer either fills or empties, a controlled slip occurs. If the buffer empties, a full frame of data is repeated at RSER and the [RLS4.5](#) and [RLS4.6](#) bits are set to 1. If the buffer fills, a full frame of data is deleted and the [RLS4.5](#) and [RLS4.7](#) bits are set to 1.

8.8.1.6 Receiving Mapped E1 Transmit Channels from a 1.544MHz Backplane

The user can use the TSCLKM bit in [TIOCR.4](#) to enable the transmit elastic store to operate with a 1.544MHz backplane (24 channels / frame + F-bit). In this mode the user can choose which of the E1 time slots will have all-ones data inserted by programming the Transmit Blank Channel Select registers ([TBCS1:TBCS4](#)). A logic 1 in the associated bit location causes the elastic store to force all ones at the outgoing E1 data for that channel. Typically the user will want to program eight channels to be blanked. The default (power-up) configuration blanks channels 25 to 32, so that the first 24 E1 channels are mapped from the 24 channels of the 1.544MHz backplane.

8.8.1.7 Mapping E1 Channels onto a 1.544MHz Backplane

The user can use the RSCLKM bit ([RIOCR.4](#)) to enable the receive elastic store to operate with a 1.544MHz backplane (24 channels / frame + F-bit). In this mode the user can choose which of the E1 time slots will be ignored (not transmitted onto RSER) by programming the Receive Blank Channel Select registers ([RBCS1:RBCS4](#)). A logic 1 in the associated bit location causes the elastic store to ignore the incoming E1 data for that channel. Typically the user will want to program eight channels to be ignored. The default (power-up) configuration will ignore channels 25 to 32, so that the first 24 E1 channels are mapped into the 24 channels of the 1.544MHz backplane. In this mode the F-bit location at RSER is always set to 1.

For example, if the user wants to ignore E1 time slots 0 (channel 1) and TS16 (channel 17), the [RBCS1:RBCS4](#) registers would be programmed as follows:

[RBCS1](#) = 01h
[RBCS2](#) = 00h
[RBCS3](#) = 01h
[RBCS4](#) = FCh

8.8.2 IBO Multiplexer

The Interleaved Bus Operation (IBO) multiplexer is used in conjunction with the IBO function located within each framer/formatter block (controlled by the [RIBOC](#) and [TIBOC](#) registers). When enabled, the IBO multiplexer simplifies user interface by connecting bus signals internally. The IBO multiplexer eliminates the need for ganged external wiring and tri-state output drivers on the RSER and RSIG pins. This option provides a more controlled, cleaner, and lower power mode of operation.

Note that the channel block signals TCHBLK and RCHBLK are output at the rate of the of IBO selection. Hence, a 4.096MHz IBO would have the channel blocks (if programmed active at the rate of 4.096MHz). The particular blocking channel would be active for a duration of the channel if programmed.

The DS26524 also supports the traditional mode of IBO operation by allowing complete access to individual framers, and tri-stating the RSER and RSIG pins at the appropriate times for external bus wiring. This mode of operation is enabled per framer in the associated [RIBOC](#) and [TIBOC](#) registers, while leaving the IBO multiplexer is disabled (IBOMS0 = 0 and IBOMS1 = 0).

[Figure 8-3](#), [Figure 8-4](#), and [Figure 8-5](#) show the equivalent internal circuit for each IBO mode. [Table 8-4](#) describes the pin function changes for each mode of the IBO multiplexer.

Table 8-4. Registers Related to the IBO Multiplexer

| REGISTER | FRAMER ADDRESSES | FUNCTION |
|--|------------------|--|
| Global Transceiver Control Register 1 (GTCR1) | 0F0h | This is a global register for all four framers. It can be used to specify ganged operation for the IBO. |
| Receive Interleave Bus Operation Control Register (RIBOC) | 088h | This register can be used for control of how many framers and the corresponding speed for the IBO links for the receiver. |
| Transmit Interleave Bus Operation Control Register (TIBOC) | 188h | This register can be used for control of how many framers and the corresponding speed for the IBO links for the transmitter. |

Note: The addresses shown are for Framer 1. Addresses for Framers 2 to 4 can be calculated by using the following: Framer n = (Framer 1 address + (n - 1) x 200h), where n = 2 to 4 for Framers 2 to 4.

Figure 8-3. IBO Multiplexer Equivalent Circuit—4.096MHz

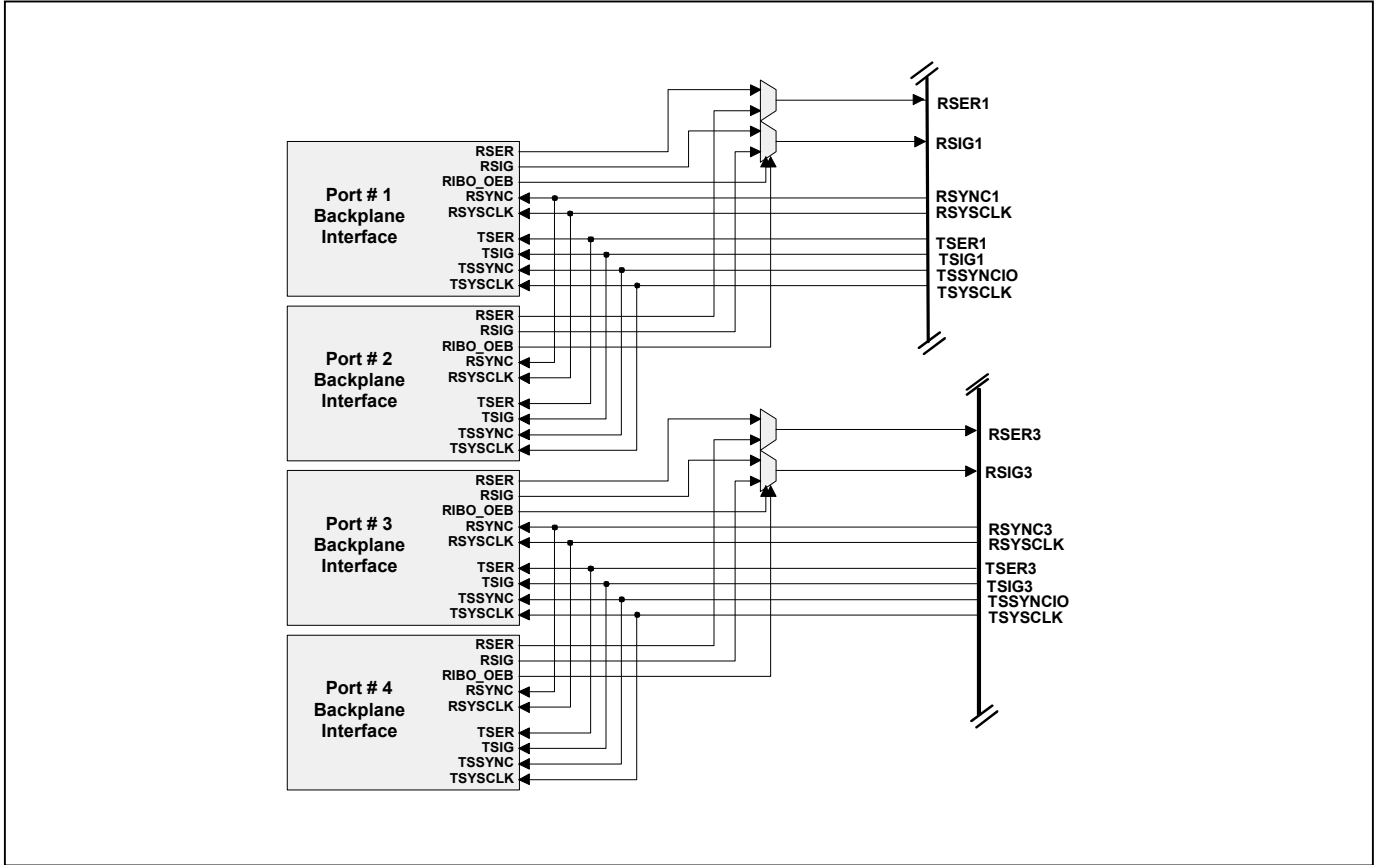


Figure 8-4. IBO Multiplexer Equivalent Circuit—8.192MHz

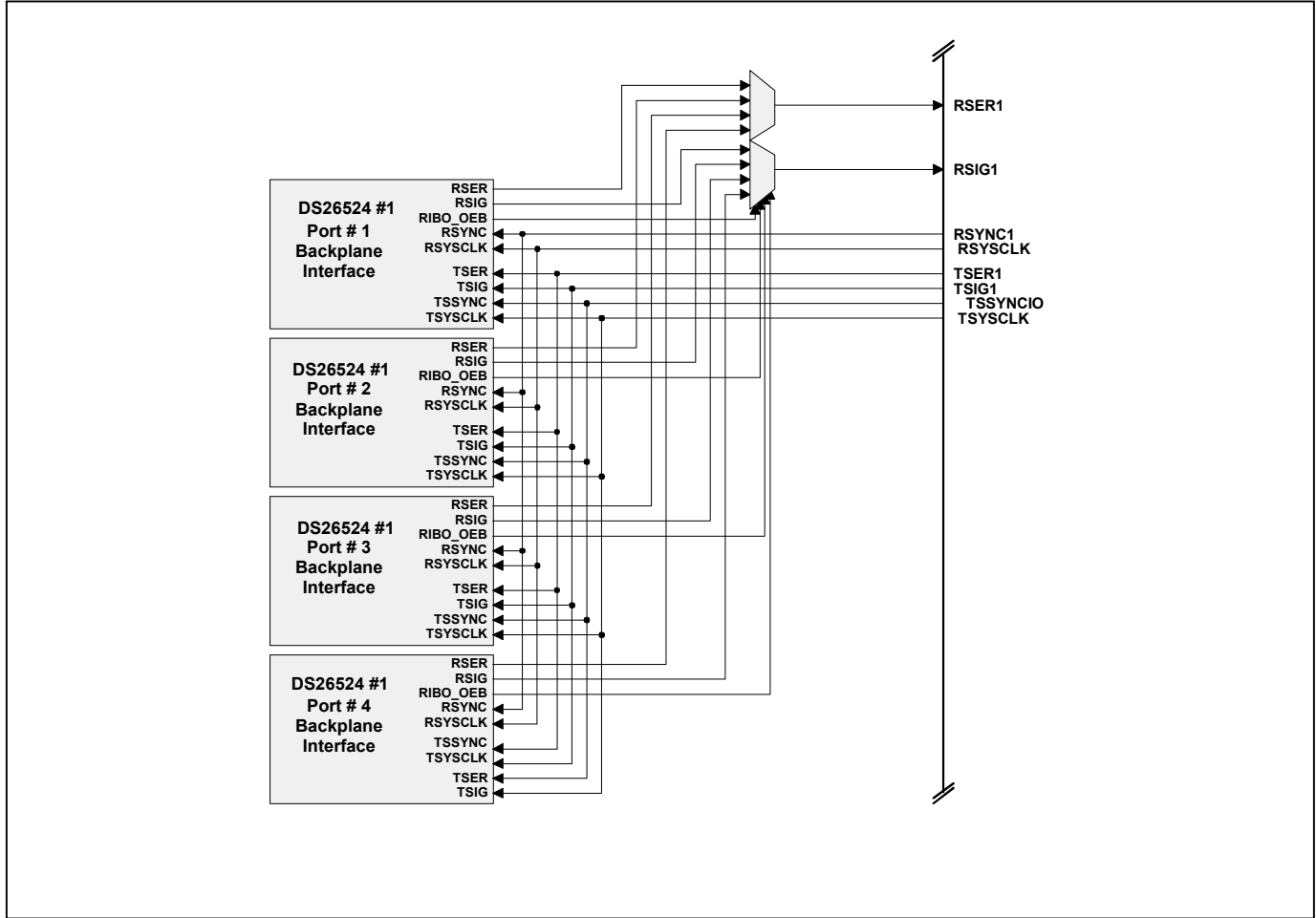


Figure 8-5. IBO Multiplexer Equivalent Circuit—16.384MHz

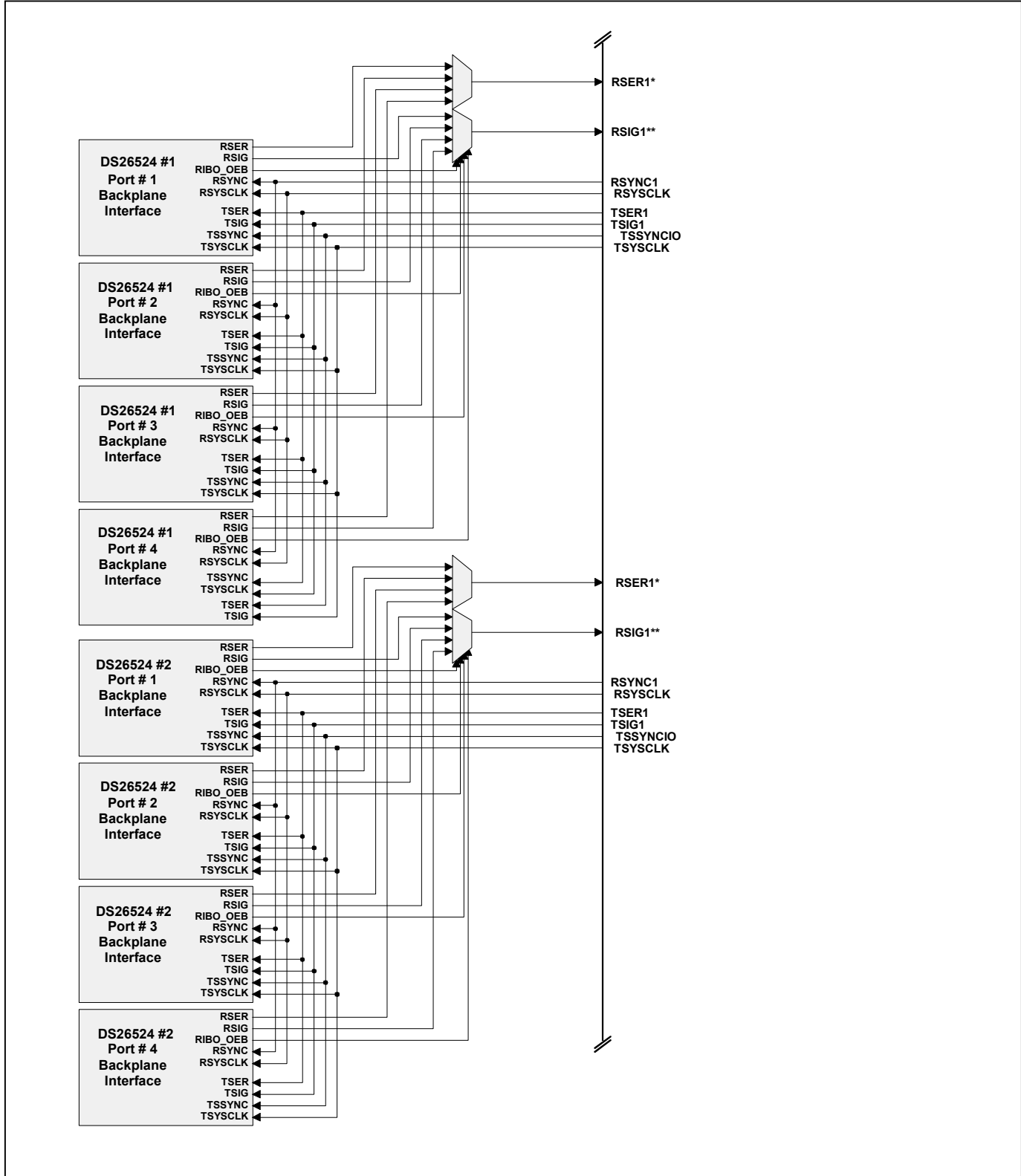


Table 8-5. RSER Output Pin Definitions

| PIN | NORMAL USE | 4.096MHz IBO | 8.192MHz IBO | 16.384MHz IBO |
|------------|--------------------------------|--|--|-----------------------------------|
| RSER1 | Receive Serial Data for Port 1 | Combined Receive Serial Data for Ports 1 and 2 | Combined Receive Serial Data for Ports 1–4 | Receive Serial Data for Ports 1–4 |
| RSER2 | Receive Serial Data for Port 2 | Reserved | Unused | Unused |
| RSER3 | Receive Serial Data for Port 3 | Combined Receive Serial Data for Ports 3 and 4 | Unused | Unused |
| RSER4 | Receive Serial Data for Port 4 | Unused | Unused | Unused |

Table 8-6. RSIG Output Pin Definitions

| PIN | NORMAL USE | 4.096MHz IBO | 8.192MHz IBO | 16.384MHz IBO |
|------------|-----------------------------------|---|---|--------------------------------------|
| RSIG1 | Receive Signaling Data for Port 1 | Combined Receive Signaling Data for Ports 1 and 2 | Combined Receive Signaling Data for Ports 1–4 | Receive Signaling Data for Ports 1–4 |
| RSIG2 | Receive Signaling Data for Port 2 | Unused | Unused | Unused |
| RSIG3 | Receive Signaling Data for Port 3 | Combined Receive Signaling Data for Ports 3 and 4 | Unused | Unused |
| RSIG4 | Receive Signaling Data for Port 4 | Unused | Unused | Unused |

Table 8-7. TSER Input Pin Definitions

| PIN | NORMAL USE | 4.096MHz IBO | 8.192MHz IBO | 16.384MHz IBO |
|-------|---------------------------------|---|---|------------------------------------|
| TSER1 | Transmit Serial Data for Port 1 | Combined Transmit Serial Data for Ports 1 and 2 | Combined Transmit Serial Data for Ports 1–4 | Transmit Serial Data for Ports 1–4 |
| TSER2 | Transmit Serial Data for Port 2 | Unused | Unused | Unused |
| TSER3 | Transmit Serial Data for Port 3 | Combined Transmit Serial Data for Ports 3 and 4 | Unused | Unused |
| TSER4 | Transmit Serial Data for Port 4 | Unused | Unused | Unused |

Table 8-8. TSIG Input Pin Definitions

| PIN | NORMAL USE | 4.096MHz IBO | 8.192MHz IBO | 16.384MHz IBO |
|-------|------------------------------------|--|--|---------------------------------------|
| TSIG1 | Transmit Signaling Data for Port 1 | Combined Transmit Signaling Data for Ports 1 and 2 | Combined Transmit Signaling Data for Ports 1–4 | Transmit Signaling Data for Ports 1–4 |
| TSIG2 | Transmit Signaling Data for Port 2 | Unused | Unused | Unused |
| TSIG3 | Transmit Signaling Data for Port 3 | Combined Transmit Signaling Data for Ports 3 and 4 | Unused | Unused |
| TSIG4 | Transmit Signaling Data for Port 4 | Unused | Unused | Unused |

Table 8-9. RSYNC Input Pin Definitions

| PIN | NORMAL USE | 4.096MHz IBO | 8.192MHz IBO | 16.384MHz IBO |
|--------|--------------------------------|---------------------------------------|-----------------------------------|-----------------------------------|
| RSYNC1 | Receive Frame Pulse for Port 1 | Receive Frame Pulse for Ports 1 and 2 | Receive Frame Pulse for Ports 1–4 | Receive Frame Pulse for Ports 1–4 |
| RSYNC2 | Receive Frame Pulse for Port 2 | Unused | Unused | Unused |
| RSYNC3 | Receive Frame Pulse for Port 3 | Receive Frame Pulse for Ports 3 and 4 | Unused | Unused |
| RSYNC4 | Receive Frame Pulse for Port 4 | Unused | Unused | Unused |

8.8.3 H.100 (CT Bus) Compatibility

The registers used for controlling the H.100 backplane are [RIOCR](#) and [TIOCR](#).

The H.100 (or CT bus) is a synchronous, bit-serial, TDM transport bus operating at 8.192MHz. The H.100 standard also allows compatibility modes to operate at 2.048MHz, 4.096MHz, or 8.192MHz. The control bit H100EN ([RIOCR.5](#)), when combined with RSYNCINV and TSSYNCINV, allows the DS26524 to accept a CT bus-compatible frame-sync signal ([CT_FRAME](#)) at the RSYNC and TSSYNCIO (input mode) inputs.

The following rules apply to the H100EN control bit.

- 1) The H100EN bit controls the sampling point for the RSYNC (input mode) and TSSYNCIO (input mode) only. The RSYNC output and other sync signals are not affected.
- 2) The H100EN bit would always be used in conjunction with the receive and transmit elastic store buffers.
- 3) The H100EN bit would typically be used with 8.192MHz IBO mode, but could also be used with 4.096MHz IBO mode or 2.048MHz backplane operation.
- 4) The H100EN bit in RIOCR controls both RSYNC and TSSYNCIO (i.e., there is no separate control bit for the TSSYNCIO).
- 5) The H100EN bit does *not* invert the expected signal; RSYNCINV ([RIOCR](#)) and TSSYNCINV ([TIOCR](#)) must be set high to invert the inbound sync signals.

Figure 8-6. RSYNC Input in H.100 (CT Bus) Mode

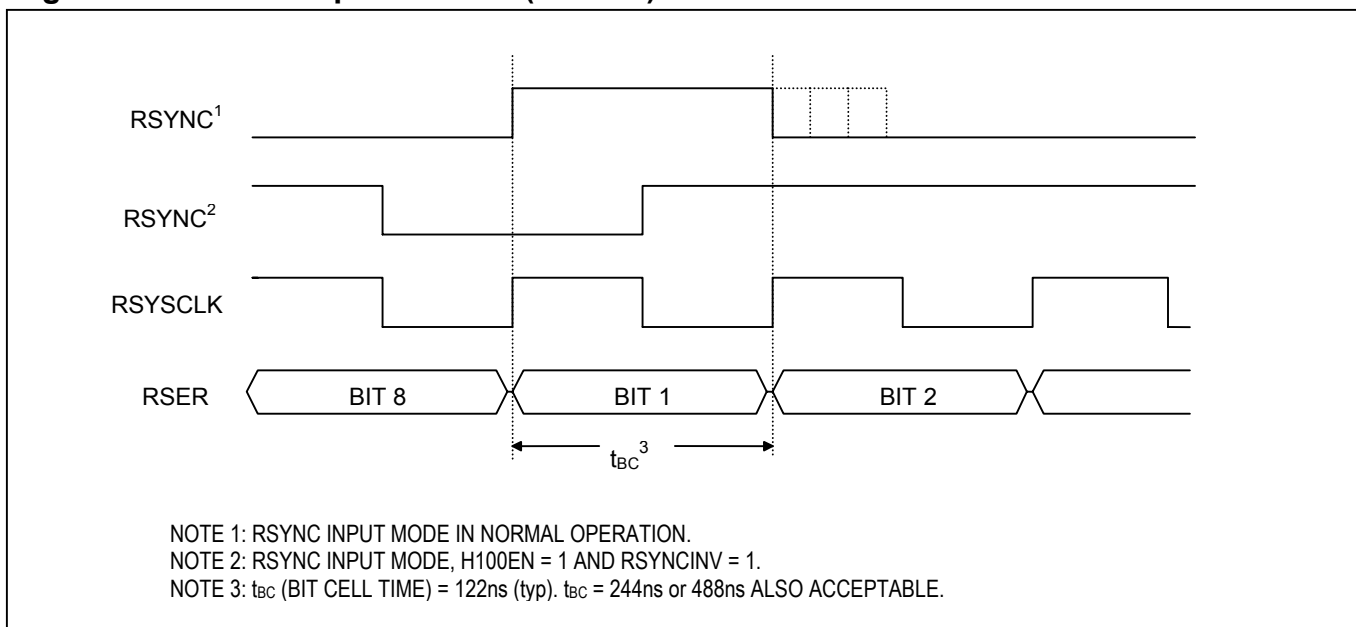
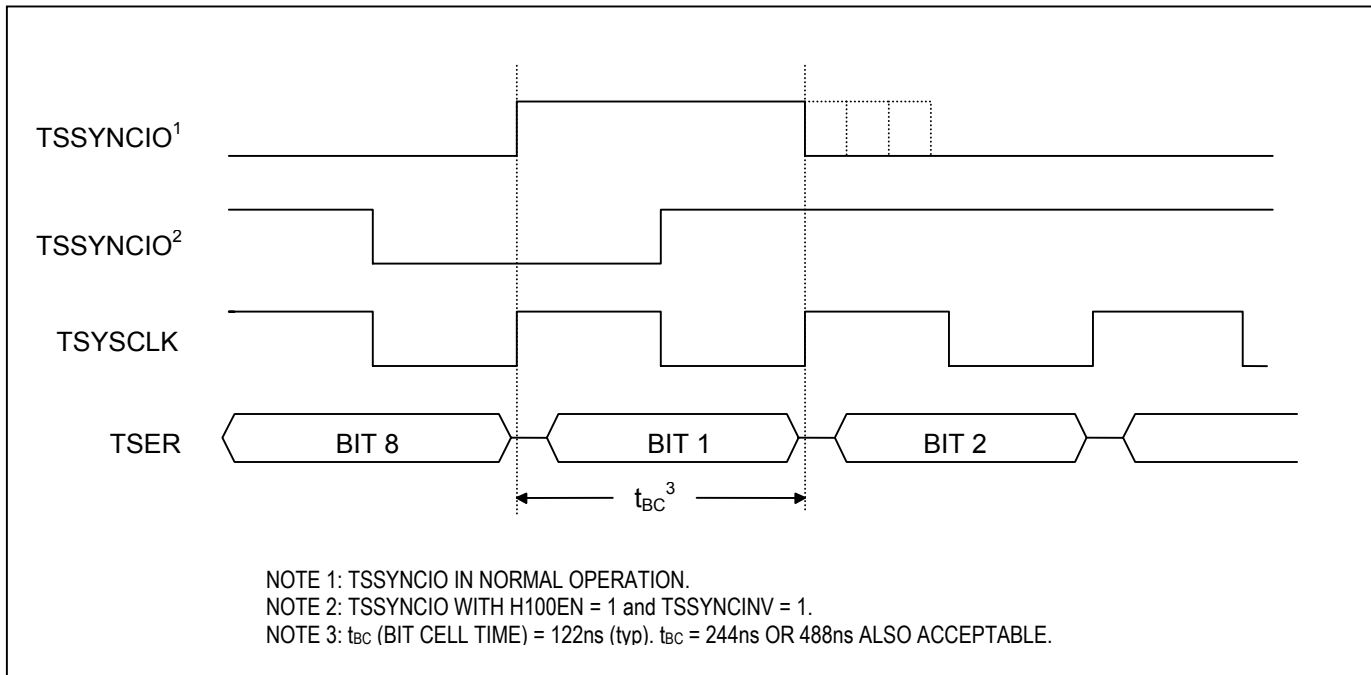


Figure 8-7. TSSYNCIO (Input Mode) Input in H.100 (CT Bus) Mode

8.8.4 Receive and Transmit Channel Blocking Registers

The Receive Channel Blocking registers ([RCBR1:RCBR4](#)) and the Transmit Channel Blocking registers ([TCBR1:TCBR4](#)) control the RCHBLK and TCHBLK pins, respectively. The RCHBLK and TCHBLK pins are user-programmable outputs that can be forced either high or low during individual channels. These outputs can be used to block clocks to a USART or LAPD controller in ISDN-PRI applications. When the appropriate bits are set to 1, the RCHBLK and TCHBLK pins are held high during the entire corresponding channel time. When used with a T1 (1.544MHz) backplane, only [TCBR1:TCBR2:TCBR3](#) are used. [TCBR4](#) is included to support an E1 (2.048MHz) backplane when the elastic store is configured for T1-to-E1 rate conversion. See Section [8.8.1](#).

8.8.5 Transmit Fractional Support (Gapped Clock Mode)

The DS26524 can be programmed to output gapped clocks for selected channels in the receive and transmit paths to simplify connections into a USART or LAPD controller in fractional T1/E1 or ISDN-PRI applications. When the gapped clock feature is enabled, a gated clock is output on the TCHCLK signal. The channel selection is controlled via the Transmit Gapped-Clock Channel Select registers ([TGCCS1:TGCCS4](#)). The transmit path is enabled for gapped clock mode with the TGCLKEN bit ([TESCR.6](#)). Both 56kbps and 64kbps channel formats are supported as determined by [TESCR.7](#). When 56kbps mode is selected, the clock corresponding to the data/control bit in the channel is omitted (only the seven most significant bits of the channel have clocks).

8.8.6 Receive Fractional Support (Gapped Clock Mode)

The DS26524 can be programmed to output gapped clocks for selected channels in the receive and transmit paths to simplify connections into a USART or LAPD controller in fractional T1/E1 or ISDN-PRI applications. When the gapped clock feature is enabled, a gated clock is output on the RCHCLK signal. The channel selection is controlled via the Receive Gapped-Clock Channel Select registers ([RGCCS1:RGCCS4](#)). The receive path is enabled for gapped clock mode with the RGCLKEN bit ([RESOCR.6](#)). Both 56kbps and 64kbps channel formats are supported as determined by [RESOCR.7](#). When 56kbps mode is selected, the clock corresponding to the data/control bit in the channel is omitted (only the seven most significant bits of the channel have clocks).

8.9 Framers

The DS26524 framer cores are software selectable for T1, J1, or E1. The receive framer locates the frame and multiframe boundaries and monitors the data stream for alarms. It is also used for extracting and inserting signaling data, T1 FDL data, and E1 Si- and Sa-bit information. The receive-side framer decodes AMI, B8ZS line coding, synchronizes to the data stream, reports alarm information, counts framing/coding and CRC errors, and provides clock/data and frame-sync signals to the backplane interface section. Diagnostic capabilities include loopbacks, and 16-bit loop-up and loop-down code detection. The device contains a set of internal registers for host access and control of the device.

On the transmit side, clock, data, and frame-sync signals are provided to the framer by the backplane interface section. The framer inserts the appropriate synchronization framing patterns, alarm information, calculates and inserts the CRC codes, and provides the B8ZS (zero code suppression) and AMI line coding.

Both the transmit and receive path have an HDLC controller. The HDLC controller transmits and receives data via the framer block. The HDLC controller can be assigned to any time slot, portion of a time slot, or to FDL (T1). The HDLC controller has separate 64-byte Tx and Rx FIFO to reduce the amount of processor overhead required to manage the flow of data.

The backplane interface provides a versatile method of sending and receiving data from the host system. Elastic stores provide a method for interfacing to asynchronous systems, converting from a T1/E1 network to a 2.048MHz, 4.096MHz, 8.192MHz, or N x 64kHz system backplane. The elastic stores also manage slip conditions (asynchronous interface). An IBO is provided to allow multiple framers in the DS26524 to share a high-speed backplane.

8.9.1 T1 Framing

DS1 trunks contain 24 bytes of serial voice/data channels bundled with an overhead bit, the F-bit. The F-bit contains a fixed pattern for the receiver to delineate the frame boundaries. The F-bit is inserted once per frame at the beginning of the transmit frame boundary. The frames are further grouped into bundles of frames 12 for D4 and 24 for ESF.

The D4 and ESF framing modes are outlined in [Table 8-10](#) and [Table 8-11](#). In the D4 mode, framing bit for frame 12 is ignored if Japanese Yellow is selected.

Table 8-10. D4 Framing Mode

| FRAME NUMBER | Ft | Fs | SIGNALING |
|--------------|----|----|-----------|
| 1 | 1 | | |
| 2 | | 0 | |
| 3 | 0 | | |
| 4 | | 0 | |
| 5 | 1 | | |
| 6 | | 1 | A |
| 7 | 0 | | |
| 8 | | 1 | |
| 9 | 1 | | |
| 10 | | 1 | |
| 11 | 0 | | |
| 12 | | 0 | B |

Table 8-11. ESF Framing Mode

| FRAME NUMBER | FRAMING | FDL | CRC | SIGNALING |
|--------------|---------|-----|-------|-----------|
| 1 | | √ | | |
| 2 | | | CRC-1 | |
| 3 | | √ | | |
| 4 | 0 | | | |
| 5 | | √ | | |
| 6 | | | CRC-2 | √ |
| 7 | | √ | | |
| 8 | 0 | | | |
| 9 | | √ | | |
| 10 | | | CRC-3 | |
| 11 | | √ | | |
| 12 | | | | √ |
| 13 | | √ | | |
| 14 | | | CRC-4 | |
| 15 | | √ | | |
| 16 | 0 | | | |
| 17 | | √ | | √ |
| 18 | | | CRC-5 | |
| 19 | | √ | | |
| 20 | 1 | | | |
| 21 | | √ | | |
| 22 | | | CRC-6 | |
| 23 | | √ | | |
| 24 | 1 | | | √ |

Table 8-12. SLC-96 Framing

| FRAME NUMBER | Ft | Fs | SIGNALING |
|--------------|----|----|-----------|
| 1 | 1 | | |
| 2 | | 0 | |
| 3 | 0 | | |
| 4 | | 0 | |
| 5 | 1 | | |
| 6 | | 1 | A |
| 7 | 0 | | |
| 8 | | 1 | |
| 9 | 1 | | |
| 10 | | 1 | |
| 11 | 0 | | |
| 12 | | 0 | B |
| 13 | 1 | | |
| 14 | | 0 | |
| 15 | 0 | | |
| 16 | | 0 | |
| 17 | 1 | | |
| 18 | | 1 | C |
| 19 | 0 | | |
| 20 | | 1 | |
| 21 | 1 | | |
| 22 | | 1 | |
| 23 | 0 | | |

| FRAME NUMBER | Ft | Fs | SIGNALING |
|--------------|----|------------------------|-----------|
| 24 | | C1 (Concentrator Bit) | D |
| 25 | 1 | | |
| 26 | | C2 (Concentrator Bit) | |
| 27 | 0 | | |
| 28 | | C3 (Concentrator Bit) | |
| 29 | 1 | | |
| 30 | | C4 (Concentrator Bit) | A |
| 31 | 0 | | |
| 32 | | C5 (Concentrator Bit) | |
| 33 | 1 | | |
| 34 | | C6 (Concentrator Bit) | |
| 35 | 0 | | |
| 36 | | C7 (Concentrator Bit) | B |
| 37 | 1 | | |
| 38 | | C8 (Concentrator Bit) | |
| 39 | 0 | | |
| 40 | | C9 (Concentrator Bit) | |
| 41 | 1 | | |
| 42 | | C10 (Concentrator Bit) | C |
| 43 | 0 | | |
| 44 | | C11 (Concentrator Bit) | |
| 45 | 1 | | |
| 46 | | 0 (Spoiler Bit) | |
| 47 | 0 | | D |
| 48 | | 1 (Spoiler Bit) | |
| 49 | 1 | | |
| 50 | | 0 (Spoiler Bit) | |
| 51 | 0 | | |
| 52 | | M1 (Maintenance Bit) | |
| 53 | 1 | | |
| 54 | | M2 (Maintenance Bit) | A |
| 55 | 0 | | |
| 56 | | M3 (Maintenance Bit) | |
| 57 | 1 | | |
| 58 | | A1 (Alarm Bit) | |
| 59 | 0 | | |
| 60 | | A2 (Alarm Bit) | B |
| 61 | 1 | | |
| 62 | | S1 (Switch Bit) | |
| 63 | 0 | | |
| 64 | | S2 (Switch Bit) | |
| 65 | 1 | | C |
| 66 | | S3 (Switch Bit) | |
| 67 | 0 | | |
| 68 | | S4 (Switch Bit) | |
| 69 | 1 | | |
| 70 | | 1 (Spoiler Bit) | |
| 71 | 0 | | |
| 72 | | 0 | D |

8.9.2 E1 Framing

The E1 framing consists of FAS, NFAS detection as shown in [Table 8-13](#).

Table 8-13. E1 FAS/NFAS Framing

| CRC-4 FRAME # | TYPE | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---------------|------|----|---|---|-----|-----|-----|-----|-----|
| 0 | FAS | C1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | NFAS | 0 | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| 2 | FAS | C2 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 3 | NFAS | 0 | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| 4 | FAS | C3 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 5 | NFAS | 1 | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| 6 | FAS | C4 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 7 | NFAS | 0 | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| 8 | FAS | C1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 9 | NFAS | 1 | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| 10 | FAS | C2 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 11 | NFAS | 1 | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| 12 | FAS | C3 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 13 | NFAS | E1 | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| 14 | FAS | C4 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 15 | NFAS | E2 | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |

C = C bits are the CRC-4 remainder, A = alarm bits, Sa = bits for data link.

[Table 8-14](#) shows registers that are related to setting up the framing.

Table 8-14. Registers Related to Setting Up the Framer

| REGISTER | FRAMER ADDRESSES | FUNCTION |
|--|------------------|---|
| Transmit Master Mode Register (TMMR) | 180h | T1/E1 mode. |
| Transmit Control Register 1 (TCR1) | 181h | Source of the F-bit. |
| Transmit Control Register 2 (TCR2) | 182h | F-bit corruption, selection of SLC-96. |
| Transmit Control Register 3 (TCR3) | 183h | ESF or D4 mode selection. |
| Receive Master Mode Register (RMMR) | 080h | T1/E1 selection for receiver. |
| Receive Control Register 1 (RCR1) | 081h | Resynchronization criteria for the framer. |
| Receive Control Register 2 (T1RCR2) | 014h | T1 remote alarm and OOF criteria. |
| Receive Control Register 2 (E1RCR2) | 082h | E1 receive loss of signal criteria selection. |
| Receive Latched Status Register 1 (RLS1) | 090h | Receive latched status 1. |
| Receive Interrupt Mask Register 1 (RIM1) | 0A0h | Receive interrupt mask 1. |
| Receive Latched Status Register 2 (RLS2) | 091h | Receive latched status 2. |
| Receive Interrupt Mask Register 2 (RIM2) | 0A1h | Receive interrupt mask 2. |
| Receive Latched Status Register 4 (RLS4) | 093h | Receive latched status 4. |
| Receive Interrupt Mask Register 4 (RIM4) | 0A3h | Receive interrupt mask 4. |
| Frames Out of Sync Count Register 1 (FOSCR1) | 054h | Framer out of sync register 1. |
| Frames Out of Sync Count Register 2 (FOSCR2) | 055h | Framer out of sync register 2. |
| E1 Receive Align Frame Register (E1RAF) | 064h | RAF byte. |
| E1 Receive Non-Align Frame Register (E1RNAF) | 065h | RNAF byte. |
| Transmit SLC-96 Data Link Register 1 (T1TSLC1) | 164h | Transmit SLC-96 bits. |
| Transmit SLC-96 Data Link Register 2 (T1TSLC2) | 165h | Transmit SLC-96 bits. |
| Transmit SLC-96 Data Link Register 3 (T1TSLC3) | 166h | Transmit SLC-96 bits. |
| Receive SLC-96 Data Link Register 1 (T1RSLC1) | 064h | Receive SLC-96 bits. |
| Receive SLC-96 Data Link Register 2 (T1RSLC2) | 065h | Receive SLC-96 bits. |
| Receive SLC-96 Data Link Register 3 (T1RSLC3) | 066h | Receive SLC-96 bits. |

Note: The addresses shown are for Framer 1. Addresses for Framers 2 to 4 can be calculated using the following: Framer n = (Framer 1 address + $(n - 1) \times 200h$); where $n = 2$ to 4 for Framers 2 to 4.

8.9.3 T1 Transmit Synchronizer

The DS26524 transmitter can identify the D4 or ESF frame boundary, as well as the CRC multiframe boundaries within the incoming NRZ data stream at TSER. The TFM ([TCR3.2](#)) control bit determines whether the transmit synchronizer searches for the D4 or ESF multiframe. Additional control signals for the transmit synchronizer are located in the [TSYNCC](#) register. The latched status bit [TLS3.0](#) (LOFD) is provided to indicate that a loss-of-frame synchronization has occurred. The real-time bit (LOF) is also provided to indicate when the synchronizer is searching for frame/multiframe alignment. The LOFD bit can be enabled to cause an interrupt condition on [INTB](#).

Note that when the transmit synchronizer is used, the TSYNC signal should be set as an output (TSIO = 1) and the recovered frame-sync pulse will be output on this signal. The recovered CRC-4 multiframe sync pulse is output if enabled with [TIOCR.0](#) (TSM = 1).

Other key points concerning the E1 transmit synchronizer:

- 1) The Tx synchronizer is not operational when the transmit elastic store is enabled, including IBO modes.
- 2) The Tx synchronizer does not perform CRC-6 alignment verification (ESF mode) and does not verify CRC-4 codewords.

The Tx synchronizer cannot search for the CAS multiframe. [Table 8-15](#) shows the registers related to the transmit synchronizer.

Table 8-15. Registers Related to the Transmit Synchronizer

| REGISTER | FRAMER ADDRESSES | FUNCTION |
|---|------------------|---|
| Transmit Synchronizer Control Register (TSYNCC) | 18Eh | Resynchronization control for the transmit synchronizer. |
| Transmit Control Register 3 (TCR3) | 183h | TFM bit selects between D4 and ESF for the transmit synchronizer. |
| Transmit Latched Status Register 3 (TLS3) | 192h | Provides latched status for the transmit synchronizer. |
| Transmit Interrupt Mask Register 3 (TIM3) | 1A2h | Provides mask bits for the TLS3 status. |
| Transmit I/O Configuration Register (TIOCR) | 184h | TSYNC should be set as an output. |

Note: The addresses shown are for Framer 1. Addresses for Framers 2 to 4 can be calculated using the following: Framer n = (Framer 1 address + $(n - 1) \times 200h$); where $n = 2$ to 4 for Framers 2 to 4.

8.9.4 Signaling

The DS26524 supports both software- and hardware-based signaling. Interrupts can be generated on changes of signaling data. The DS26524 is also equipped with receive-signaling freeze on loss of synchronization (OOF), carrier loss, or change of frame alignment. The DS26524 also has hardware pins to indicate signaling freeze.

- Flexible signaling support
 - Software or hardware based
 - Interrupt generated on change of signaling data
 - Receive-signaling freeze on loss of frame, loss of signal, or change of frame alignment
- Hardware pins for carrier loss and signaling freeze indication

Table 8-16. Registers Related to Signaling

| REGISTER | FRAMER ADDRESSES | FUNCTION |
|---|---|--|
| Transmit-Signaling Registers 1 to 16 (TS1 to TS16) | 140h to 14Bh (T1/J1) 140h to 14Fh (E1 CAS) | Transmit ABCD signaling. |
| Software-Signaling Insertion Enable Registers 1 to 4 (SSIE1 to SSIE4) | 118h, 119h, 11Ah, 11Bh | When enabled, signaling is inserted for the channel. |
| Transmit Hardware-Signaling Channel Select Registers 1 to 4 (THSCS1 to THSCS4) | 1C8h, 1C9h, 1CAh, 1CBh | Bits determine which channels will have signaling inserted in hardware-signaling mode. |
| Receive-Signaling Control Register (RSIGC) | 013h | Freeze control for receive signaling. |
| Receive-Signaling All-Ones Insertion Registers 1 to 3 (T1RSAOI1 to T1RSAOI3) | 038h, 039h, 03Ah | Registers for all-ones insertion (T1 mode only). |
| Receive-Signaling Registers 1 to 16 (RS1 to RS16) | 040h to 04Bh (T1/J1) 040h to 04Fh (E1) | Receive-signaling bytes. |
| Receive-Signaling Status Registers 1 to 4 (RSS1 to RSS4) | 098h to 09Ah (T1/J1) 98h to 9Fh (E1) | Receive-signaling change of status bits. |
| Receive-Signaling Change of State Enable Registers 1 to 4 (RSCSE1 to RSCSE4) | 0A8h, 0A9h, 0AAh, 0ABh | Receive-signaling change of state interrupt enable. |
| Receive Latched Status Register 4 (RLS4) | 093h | Receive-signaling change of state bit. |
| Receive Interrupt Mask Register 4 (RIM4) | 0A3h | Receive-signaling change of state interrupt mask bit. |
| Receive-Signaling Reinsertion Enable Registers 1 to 4 (RSI1 to RSI4) | 0C8h, 0C9h, 0CAh, 0CBh | Registers for signaling reinsertion. |

Note: The addresses shown are for Framer 1. Addresses for Framers 2 to 4 can be calculated using the following: Framer $n = (\text{Framer 1 address} + (n - 1) \times 200h)$; where $n = 2$ to 4 for Framers 2 to 4.

8.9.4.1 Transmit-Signaling Operation

There are two methods to provide transmit-signaling data. These are processor based (i.e., software based) or hardware based. Processor based refers to access through the transmit-signaling registers, [TS1:TS16](#), while hardware based refers to using the TSIG pins. Both methods can be used simultaneously.

8.9.4.1.1 Processor-Based Signaling

In processor-based mode, signaling data is loaded into the transmit-signaling registers ([TS1:TS16](#)) via the host interface. On multiframe boundaries, the contents of these registers are loaded into a shift register for placement in the appropriate bit position in the outgoing data stream. The user can use the transmit multiframe interrupt in Latched Status Register 1 ([TLS1.2](#)) to know when to update the signaling bits. The user need not update any transmit-signaling register for which there is no change of state for that register.

Each transmit-signaling register contains the robbed-bit signaling ([TCR1.4](#) in T1 mode) or TS16 CAS signaling ([TCR1.6](#) in E1 mode) for one time slot that will be inserted into the outgoing stream. Signaling data can be sourced from the TS registers on a per-channel basis by using the software-signaling insertion enable registers, [SSIE1:SSIE4](#).

In T1 ESF framing mode, there are four signaling bits per channel (A, B, C, and D). TS1:TS12 contain a full multiframe of signaling data. In T1 D4 framing mode, there are only two signaling bits per channel (A and B). In T1 D4 framing mode, the framer uses A and B bit positions for the next multiframe. The C and D bit positions become “don’t care” in D4 mode.

In E1 mode, TS16 carries the signaling information. This information can be in either CCS (common-channel signaling) or CAS (channel-associated signaling) format. The 32 time slots are referenced by two different channel number schemes in E1. In channel numbering, TS0 to TS31 are labeled channel 1 to channel 32. In phone channel numbering, TS1 to TS15 are labeled channel 1 to channel 15, and TS17 to TS31 are labeled channel 15 to channel 30.

8.9.4.2 Time Slot Numbering Schemes

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| TS | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
| Channel | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
| Phone Channel | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 |

8.9.4.2.1 Hardware-Based Signaling

In hardware-based mode, signaling data is input via the TSIG pin. This signaling PCM stream is buffered and inserted to the data stream being input at the TSER pin.

Signaling data can be input via the transmit hardware-signaling channel select ([THSCS1](#)) function. The framer can be set up to take the signaling data presented at the TSIG pin and insert the signaling data into the PCM data stream that is being input at the TSER pin. The user can control which channels are to have signaling data from the TSIG pin inserted into them on a per-channel basis. The signaling insertion capabilities of the framer are available whether the transmit-side elastic store is enabled or disabled. If the elastic store is enabled, the backplane clock (TSYSCLK) can be either 1.544MHz or 2.048MHz.

8.9.4.3 Receive-Signaling Operation

There are two methods to access receive-signaling data and provide transmit-signaling data: processor based (i.e., software based) or hardware based. Processor based refers to access through the transmit- and receive-signaling registers, [RS1:RS16](#). Hardware based refers to the RSIG pin. Both methods can be used simultaneously.

8.9.4.3.1 Processor-Based Signaling

Signaling information is sampled from the receive data stream and copied into the receive-signaling registers, [RS1:RS16](#). The signaling information in these registers is always updated on multiframe boundaries. This function is always enabled.

8.9.4.3.2 Change of State

To avoid constant monitoring of the receive-signaling registers, the DS26524 can be programmed to alert the host when any specific channel or channels undergo a change of their signaling state. [RSCSE1:RSCSE4](#) are used to select which channels can cause a change-of-state indication. The change of state is indicated in Latched Status Register 4 ([RLS4.3](#)). If signaling integration is enabled, the new signaling state must be constant for three multiframes before a change-of-state indication is indicated. The user can enable the $\overline{\text{INTB}}$ pin to toggle low upon detection of a change in signaling by setting the interrupt mask bit [RIM4.3](#). The signaling integration mode is global and cannot be enabled on a channel-by-channel basis.

The user can identify which channels have undergone a signaling change of state by reading the receive-signaling status ([RSS1:RSS4](#)) registers. The information from these registers tells the user which RSx register to read for the new signaling data. All changes are indicated in the [RSS1:RSS4](#) registers regardless of the [RSCSE1:RSCSE4](#) registers.

8.9.4.3.3 Hardware-Based Receive Signaling

In hardware-based signaling, the signaling data can be obtained from the RSER pin or the RSIG pin. RSIG is a signaling PCM stream output on a channel-by-channel basis from the signaling buffer. The T1 robbed bit or E1 TS16 signaling data is still present in the original data stream at RSER. The signaling buffer provides signaling data to the RSIG pin and also allows signaling data to be reinserted into the original data stream in a different alignment that is determined by a multiframe signal from the RSYNC pin. In this mode, the receive elastic store can be enabled or disabled. If the receive elastic store is enabled, the backplane clock (RSYSCLK) can be either 1.544MHz or 2.048MHz. In the ESF framing mode, the ABCD signaling bits are output on RSIG in the lower nibble of each channel. The RSIG data is updated once a multiframe (3ms for T1 ESF, 1.5ms for T1 D4, 2ms for E1 CAS) unless a signaling freeze is in effect. In the D4 framing mode, the AB signaling bits are output twice on RSIG in the lower nibble of each channel. Thus, bits 5 and 6 contain the same data as bits 7 and 8, respectively, in each channel.

8.9.4.3.4 Receive-Signaling Reinsertion at RSER

In this mode, the user provides a multiframe sync at the RSYNC pin and the signaling data will be reinserted based on this alignment. In T1 mode, this results in two copies of the signaling data in the RSER data stream. The original signaling data is based on the Fs/ESF frame positions, and the realigned data is based on the user-supplied multiframe sync applied at RSYNC. In voice channels, this extra copy of signaling data is of little consequence. Reinsertion can be avoided in data channels since this feature is activated on a per-channel basis. For reinsertion, the elastic store must be enabled; for T1, the backplane clock can be either 1.544MHz or 2.048MHz. E1 signaling information cannot be reinserted into a 1.544MHz backplane.

Signaling-reinsertion mode is enabled on a per-channel basis by setting the receive-signaling reinsertion channel select bit high in the Receive-Signaling Reinsertion Enable register ([RSI1:RSI4](#)). The channels that are to have signaling reinserted are selected by writing to the [RSI1:RSI4](#) registers. In E1 mode, the user generally selects all channels or none for reinsertion.

8.9.4.3.5 Force Receive-Signaling All Ones

In T1 mode, the user can, on a per-channel basis, force the robbed-bit signaling bit positions to 1. This is done by using the T1-mode Receive-Signaling All-Ones Insertion registers ([T1RSAOI1:T1RSAOI3](#)). The user sets the channel select bit in the [T1RSAOI1:T1RSAOI3](#) registers to select the channels that are to have the signaling forced to one.

8.9.4.3.6 Receive-Signaling Freeze

The signaling data in the four multiframe signaling buffers is frozen in a known good state upon either a loss of synchronization (OOF event), carrier loss, or change of frame alignment. In T1 mode, this action meets the requirements of BellCore TR-TSY-000170 for signaling freezing. To allow this freeze action to occur, the RSFE control bit ([RSIGC.1](#)) should be set high. The user can force a freeze by setting the RSFF control bit ([RSIGC.2](#)) high. The RSIGF output pin provides a hardware indication that a freeze is in effect. The four multiframe buffer provides a three multiframe delay in the signaling bits provided at the RSIG pin (and at the RSER pin if receive-signaling reinsertion is enabled). When freezing is enabled (RSFE = 1), the signaling data is held in the last known good state until the corrupting error condition subsides. When the error condition subsides, the signaling data is held in the old state for at least an additional 9ms (4.5ms in D4 framing mode, 6ms for E1 mode) before being allowed to be updated with new signaling data.

The receive-signaling registers are frozen and not updated during a loss-of-sync condition. They will contain the most recent signaling information before the LOF occurred.

8.9.4.4 Transmit SLC-96 Operation (T1 Mode Only)

In an SLC-96-based transmission scheme, the standard Fs-bit pattern is robbed to make room for a set of message fields. The SLC-96 multiframe is made up of six D4 superframes, thus it is 72 frames long. In the 72-frame SLC-96 multiframe, 36 of the framing bits are the normal Ft pattern and the other 36 bits are divided into alarm, maintenance, spoiler, and concentrator bits, as well as 12 bits of the normal Fs pattern. Additional SLC-96 information can be found in BellCore document TR-TSY-000008. Registers related to the transmit FDL are shown in [Table 8-17](#).

Table 8-17. Registers Related to SLC-96

| REGISTER | FRAMER ADDRESSES | FUNCTION |
|--|------------------|--|
| Transmit FDL Register (T1TFDL) | 162h | For sending messages in transmit SLC-96 Ft/Fs bits. |
| Transmit SLC-96 Data Link Registers 1 to 3 (T1TSLC1:T1TSLC3) | 164h, 165h, 166h | Registers that control the SLC-96 overhead values. |
| Transmit Control Register 2 (TCR2) | 182h | Transmit control for data selection source for the Ft/Fs bits. |
| Transmit Latched Status Register 1 (TLS1) | 190h | Status bit for indicating transmission of data link buffer. |
| Receive SLC-96 Data Link Registers 1 to 3 (T1RSLC1:T1RSLC3) | 064h, 065h, 066h | — |
| Receive Latched Status Register 7 (RLS7) | 096h | Receive SLC-96 alignment event. |

Note: The addresses shown are for Framer 1. Addresses for Framers 2 to 4 can be calculated using the following: Framer $n = (\text{Framer 1 address} + (n - 1) \times 200\text{h})$; where $n = 2$ to 4 for Framers 2 to 4.

The [T1TFDL](#) register is used to insert the SLC-96 message fields. To insert the SLC-96 message using the [T1TFDL](#) register, the user should configure the DS26524 as shown:

- [TCR2.6](#) (TSLC96) = 1 Enable transmit SLC-96.
- [TCR2.7](#) (TFDLS) = 0 Source FS bits via TFDL or SLC-96 formatter.
- [TCR3.2](#) (TFM) = 1 D4 framing mode.
- [TCR1.6](#) (TFPT) = 0 Do not “pass through” TSER F-bits.

The DS26524 automatically inserts the 12-bit alignment pattern in the Fs bits for the SLC-96 data link frame. Data from [T1TSLC1:T1TSLC3](#) is inserted into the remaining Fs-bit locations of the SLC-96 multiframe. The status bit TSLC96 located at [TLS1.4](#) is set to indicate that the SLC-96 data link buffer has been transmitted and that the user should write new message data into [T1TSLC1:T1TSLC3](#). The host has 9ms after the assertion of TLS1.4 to write the registers [T1TSLC1:T1TSLC3](#). If no new data is provided in these registers, the previous values are retransmitted.

8.9.4.5 Receive SLC-96 Operation (T1 Mode Only)

In an SLC-96-based transmission scheme, the standard Fs-bit pattern is robbed to make room for a set of message fields. The SLC-96 multiframe is made up of six D4 superframes, thus it is 72 frames long. In the 72-frame SLC-96 multiframe, 36 of the framing bits are the normal Ft pattern and the other 36 bits are divided into alarm, maintenance, spoiler, and concentrator bits, as well as 12 bits of the normal Fs pattern. Additional SLC-96 information can be found in BellCore document TR-TSY-000008.

To enable the DS26524 to synchronize onto a SLC-96 pattern, the following configuration should be used:

- [RCR1.5](#) (RFM) = 1 Set to D4 framing mode.
- [RCR1.3](#) (SYNCC) = 1 Set to cross-couple Ft and Fs bits.
- [T1RCR2.4](#) (RSLC96) = 1 Enable SLC-96 synchronizer.
- [RCR1.7](#) (SYNCT) = 0 Set to minimum sync time.

The SLC-96 message bits can be extracted via the [T1RSLC1:T1RSLC3](#) registers. The status bit RSLC96 located at [RLS7.3](#) is useful for retrieving SLC-96 message data. The RSLC96 bit indicates when the framer has updated the data link registers [T1RSLC1:T1RSLC3](#) with the latest message data from the incoming data stream. Once the RSLC96 bit is set, the user has 9ms (or until the next RSLC96 interrupt) to retrieve the most recent message data from the [T1RSLC1:T1RSLC3](#) registers. Note that RSLC96 will not set if the DS26524 is unable to detect the 12-bit SLC-96 alignment pattern.

8.9.5 T1 Data Link

8.9.5.1 T1 Transmit Bit-Oriented Code (BOC) Transmit Controller

The DS26524 contains a BOC generator on the transmit side and a BOC detector on the receive side. The BOC function is available only in T1 mode. [Table 8-18](#) shows the registers related to the transmit bit-oriented code.

Table 8-18. Registers Related to T1 Transmit BOC

| REGISTER | FRAMER ADDRESSES | FUNCTION |
|---|------------------|--|
| Transmit BOC Register (T1TBOC) | 163h | Transmit bit-oriented message code register. |
| Transmit HDLC Control Register 2 (THC2) | 113h | Bit to enable sending of transmit BOC. |
| Transmit Control Register 1 (TCR1) | 181h | Determines the sourcing of the F-bit. |

Note: The addresses shown are for Framer 1. Addresses for Framers 2 to 4 can be calculated using the following: Framer n = (Framer 1 address + $(n - 1) \times 200h$); where $n = 2$ to 4 for Framers 2 to 4.

Bits 0 to 5 in the [T1TBOC](#) register contain the BOC message to be transmitted. Setting SBOC = 1 ([THC2.6](#)) causes the transmit BOC controller to immediately begin inserting the BOC sequence into the FDL bit position. The transmit BOC controller automatically provides the abort sequence. BOC messages will be transmitted as long as SBOC is set. Note that the TFPT ([TCR1.6](#)) control bit must be set to 0 for the BOC message to overwrite F-bit information being sampled on TSER.

8.9.5.1.1 To Transmit a BOC

- 1) Write 6-bit code into the [T1TBOC](#) register.
- 2) Set SBOC bit in [THC2](#) = 1.

8.9.5.2 Receive Bit-Oriented Code (BOC) Controller

The DS26524 framers contain a BOC generator on the transmit side and a BOC detector on the receive side. The BOC function is available only in T1, ESF mode in the data link bits. [Table 8-19](#) shows the registers related to the receive BOC operation.

Table 8-19. Registers Related to T1 Receive BOC

| REGISTER | FRAMER ADDRESSES | FUNCTION |
|--|------------------|---|
| Receive BOC Control Register (T1RBOCC) | 015h | Controls the receive BOC function. |
| Receive BOC Register (T1RBOC) | 063h | Receive bit-oriented message. |
| Receive Latched Status Register 7 (RLS7) | 096h | Indicates changes to the receive bit-oriented messages. |
| Receive Interrupt Mask Register 7 (RIM7) | 0A6h | Mask bits for RBOC for generation of interrupts. |

Note: The addresses shown are for Framer 1. Addresses for Framers 2 to 4 can be calculated using the following: Framer $n = (\text{Framer 1 address} + (n - 1) \times 200h)$; where $n = 2$ to 4 for Framers 2 to 4.

In ESF mode, the DS26524 continuously monitors the receive message bits for a valid BOC message. The BOC detect (BD) status bit at [RLS7.0](#) is set once a valid message has been detected for a time determined by the receive BOC filter bits RBF0 and RBF1 in the [T1RBOCC](#) register. The 6-bit BOC message is available in the [T1RBOC](#) register. Once the user has cleared the BD bit, it remains clear until a new BOC is detected (or the same BOC is detected following a BOC clear event). The BOC clear (BC) bit at [RLS7.1](#) is set when a valid BOC is no longer being detected for a time determined by the receive BOC disintegration bits RBD0 and RBD1 in the [T1RBOCC](#) register.

The BD and BC status bits can create a hardware interrupt on the $\overline{\text{INTB}}$ signal as enabled by the associated interrupt mask bits in the [RIM7](#) register.

8.9.5.3 Legacy T1 Transmit FDL

It is recommended that the DS26524's built-in BOC or HDLC controllers be used for most applications requiring access to the FDL. [Table 8-21](#) shows the registers related to control of the transmit FDL.

Table 8-20. Registers Related to T1 Transmit FDL

| REGISTER | FRAMER ADDRESSES | FUNCTION |
|--|------------------|---------------------------------------|
| Transmit FDL Register (T1TFDL) | 162h | FDL code used to insert transmit FDL. |
| Transmit Control Register 2 (TCR2) | 182h | Defines the source of the FDL. |
| Transmit Latched Status Register 2 (TLS2) | 191h | Transmit FDL empty bit. |
| Transmit Interrupt Mask Register 2 (HDLC) (TIM2) | 1A1h | Mask bit for TFDL empty. |

Note: The addresses shown are for Framer 1. Addresses for Framers 2 to 4 can be calculated using the following: Framer $n = (\text{Framer 1 address} + (n - 1) \times 200h)$; where $n = 2$ to 4 for Framers 2 to 4.

When enabled with [TCR2.7](#), the transmit section shifts out into the T1 data stream either the FDL (in the ESF framing mode) or the Fs bits (in the D4 framing mode) contained in the Transmit FDL register ([T1TFDL](#)). When a new value is written to the [T1TFDL](#), it is multiplexed serially (LSB first) into the proper position in the outgoing T1 data stream. After the full eight bits have been shifted out, the framer signals the host controller that the buffer is empty and that more data is needed by setting the [TLS2.4](#) bit to a 1. The $\overline{\text{INTB}}$ bit also toggles low if enabled via [TIM2.4](#). The user has 2ms to update the [T1TFDL](#) with a new value. If the [T1TFDL](#) is not updated, the old value in the [T1TFDL](#) is transmitted once again. Note that in this mode, no zero stuffing is applied to the FDL data. It is strongly suggested that the HDLC controller be used for FDL messaging applications.

In the D4 framing mode, the framer uses the [T1TFDL](#) register to insert the Fs framing pattern. To accomplish this, the [T1TFDL](#) register must be programmed to 1Ch and [TCR2.7](#) should be set to 0 (source Fs data from the [T1TFDL](#) register).

The Transmit FDL register ([T1TFDL](#)) contains the facility data link (FDL) information that is to be inserted on a byte basis into the outgoing T1 data stream. The LSB is transmitted first. In D4 mode, only the lower six bits are used.

8.9.5.4 Legacy T1 Receive FDL

It is recommended that the DS26524's built-in BOC or HDLC controllers be used for most applications requiring access to the FDL. [Table 8-21](#) shows the registers related to the receive FDL.

Table 8-21. Registers Related to T1 Receive FDL

| REGISTER | FRAMER ADDRESSES | FUNCTION |
|---|------------------|---|
| Receive FDL Register (T1RFDL) | 062h | FDL code used to insert transmit FDL. |
| Receive Latched Status Register 7(RLS7) | 096h | Receive FDL full bit is in this register. |
| Receive Interrupt Mask Register 7(RIM7) | 0A6h | Mask bit for RFDL full. |

Note: The addresses shown are for Framer 1. Addresses for Framers 2 to 4 can be calculated using the following: Framer n = (Framer 1 address + $(n - 1) \times 200h$); where $n = 2$ to 4 for Framers 2 to 4.

In the receive section, the recovered FDL bits or Fs bits are shifted bit-by-bit into the Receive FDL register ([T1RFDL](#)). Since the [T1RFDL](#) is 8 bits in length, it fills up every 2ms ($8 \times 250\mu s$). The framer signals an external controller that the buffer has filled via the [RLS7.2](#) bit. If enabled via [RIM7.2](#), the \overline{INTB} pin toggles low, indicating that the buffer has filled and needs to be read. The user has 2ms to read this data before it is lost. Note that no zero destuffing is applied for the data provided through the [T1RFDL](#) register. The [T1RFDL](#) reports the incoming facility data link (FDL) or the incoming Fs bits. The LSB is received first. In D4 framing mode, [T1RFDL](#) updates on multiframe boundaries and reports only the Fs bits.

8.9.6 E1 Data Link

[Table 8-22](#) shows the registers related to E1 data link.

Table 8-22. Registers Related to E1 Data Link

| REGISTER | FRAMER ADDRESSES | FUNCTION |
|--|------------------------------|---|
| E1 Receive Align Frame Register (E1RAF) | 064h | Receive frame alignment register. |
| E1 Receive Non-Align Frame Register Register (E1RNAF) | 065h | Receive non-frame alignment register. |
| E1 Received Si Bits of the Align Frame Register (E1RSiAF) | 066h | Receive Si bits of the frame alignment frames. |
| Received Si Bits of the Non-Align Frame Register (E1RSiNAF) | 067h | Receive Si bits of the non-frame alignment frames. |
| Received Sa4 to Sa8 Bits Register (E1RSa4 to E1RSa8) | 069h, 06Ah, 06Bh, 06Ch, 06Dh | Receive Sa bits. |
| Transmit Align Frame Register (E1TAF) | 164h | Transmit align frame register. |
| Transmit Non-Align Frame Register (E1TNAF) | 165h | Transmit non-align frame register. |
| Transmit Si Bits of the Align Frame Register (E1TSiAF) | 166h | Transmit Si bits of the frame alignment frames. |
| Transmit Si Bits of the Non-Align Frame Register (E1TSiNAF) | 167h | Transmit Si bits of the non-frame alignment frames. |
| Transmit Sa4 to Sa8 Bits Register (E1TSa4 to E1TSa8) | 169h, 16Ah, 16Bh, 16Ch, 16Dh | Transmit Sa4 to Sa8. |
| E1 Transmit Sa-Bit Control Register (E1TSACR) | 114h | Transmit sources of Sa control. |

Note: The addresses shown are for Framer 1. Addresses for Framers 2 to 4 can be calculated using the following: Framer n = (Framer 1 address + $(n - 1) \times 200h$); where $n = 2$ to 4 for Framers 2 to 4.

8.9.6.1 Additional E1 Receive Sa- and Si-Bit Receive Operation (E1 Mode)

The DS26524, when operated in the E1 mode, provides for access to both the Sa and the Si bits via two methods. The first involves using the internal [E1RAF/E1RNAF](#) and [E1TAF/E1TNAF](#) registers. The second method involves an expanded version of the first method.

8.9.6.1.1 Internal Register Scheme Based on Double-Frame (Method 1)

On the receive side, the [E1RAF](#) and [E1RNAF](#) registers will always report the data as it received in the Sa- and Si-bit locations. The [E1RAF](#) and [E1RNAF](#) registers are updated on align frame boundaries. The setting of the receive align frame bit in Receive Latched Status Register 2 ([RLS2.0](#)) indicates that the contents of the RAF and RNAF have been updated. The host can use the [RLS2.0](#) bit to know when to read the [E1RAF](#) and [E1RNAF](#) registers. The host has 250µs to retrieve the data before it is lost.

8.9.6.1.2 Internal Register Scheme Based on CRC-4 Multiframe (Receive Side)

On the receive side there is a set of eight registers ([E1RSiAF](#), [E1RSiNAF](#), [E1RRA](#), [E1RSa4:E1RSa8](#)) that report the Si and Sa bits as they are received. These registers are updated with the setting of the receive CRC-4 multiframe bit in Receive Latched Status Register 2 ([RLS2.1](#)). The host can use the [RLS2.1](#) bit to know when to read these registers. The user has 2ms to retrieve the data before it is lost. See the register descriptions for additional information.

8.9.6.1.3 Internal Register Scheme Based on CRC-4 Multiframe (Transmit Side)

On the transmit side there is a set of eight registers ([E1TSiAF](#), [E1TSiNAF](#), [E1TRA](#), [E1TSa4:E1TSa8](#)) that, via the Transmit Sa-Bit Control register ([E1TSACR](#)), can be programmed to insert both Si and Sa data. Data is sampled from these registers with the setting of the transmit multiframe bit in Transmit Latched Status Register 1 ([TLS1.3](#)). The host can use the [TLS1.3](#) bit to know when to update these registers. It has 2ms to update the data or else the old data will be retransmitted. See the register descriptions for additional information.

8.9.6.2 Sa-Bit Monitoring and Reporting

In addition to the registers outlined above, the DS26524 provides status and interrupt capability in order to detect changes in the state of selected Sa bits. The [E1RSAIMR](#) register can be used to select which Sa bits are monitored for a change of state. When a change of state is detected in one of the enabled Sa-bit positions, a status bit is set in the [RLS7](#) register via the SaXCD bit (bit 0). This status bit can, in turn, be used to generate an interrupt by unmasking [RIM7.0](#) (SaXCD). If multiple Sa bits have been enabled, the user can read the [SaBITS](#) register at address 06Eh to determine the current value of each Sa bit.

For the Sa6 bits, additional support is available to detect specific codewords per ETS 300 233. The [Sa6CODE](#) register reports the received Sa6 codeword. The codeword must be stable for a period of three submultiframes and be different from the previous stored value in order to be updated in this register. See the [Sa6CODE](#) register description for further details on the operation of this register and the values reported in it. An additional status bit is provided in [RLS7](#) (Sa6CD) to indicate if the received Sa6 codeword has changed. A mask bit is provided for this status bit in [RIM7](#) to allow for interrupt generation when enabled.

8.9.7 Maintenance and Alarms

The DS26524 provides extensive functions for alarm detection and generation. It also provides diagnostic functions for monitoring of performance and sending of diagnostic information such as the following:

- Real-time and latched status bits, interrupts, and interrupt mask for transmitter and receiver
- LOS detection
- RIA detection and generation
- PDV violation detection
- Error counters
- DS0 monitoring
- Milliwatt generation and detection
- Slip buffer status for transmit and receive

[Table 8-23](#) shows some of the registers related to maintenance and alarms.

Table 8-23. Registers Related to Maintenance and Alarms

| REGISTER | FRAMER ADDRESSES | FUNCTION |
|--|------------------|---|
| Receive Real-Time Status Register 1 (RRTS1) | 0B0h | Real-time receive status 1. |
| Receive Interrupt Mask Register 1(RIM1) | 0A0h | Real-time interrupt mask 1. |
| Receive Latched Status Register 2 (RLS2) | 091h | Real-time latched status 2. |
| Receive Real-Time Status Register 3 (RRTS3) | 0B2h | Real-time receive status 2. |
| Receive Latched Status Register 3 (RLS3) | 092h | Real-time latched status 3. |
| Receive Interrupt Mask Register 3 (RIM3) | 0A2h | Real-time interrupt mask 3. |
| Receive Interrupt Mask Register 4 (RIM4) | 0A3h | Real-time interrupt mask 3. |
| Receive Latched Status Register 7 (RLS7) | 096h | Real-time latched status 7. |
| Receive Interrupt Mask Register 7 (RIM7) | 0A6h | Real-time interrupt mask 7. |
| Transmit Latched Status Register 1 (TLS1) | 190h | Loss of transmit clock status, TPDV, etc. |
| Transmit Latched Status Register 3 (Synchronizer) (TLS3) | 192h | Loss of frame status. |
| Receive DS0 Monitor Register (RDS0M) | 060h | Receive DS0 monitor. |
| Error-Counter Configuration Register (ERCNT) | 086h | Configuration of the error counters. |
| Line Code Violation Count Register 1 (LCVCR1) | 050h | Line code violation counter 1. |
| Line Code Violation Count Register 2 (LCVCR2) | 051h | Line code violation counter 2. |
| Path Code Violation Count Register 1 (PCVCR1) | 052h | Receive path code violation counter 1. |
| Path Code Violation Count Register 2 (PCVCR2) | 053h | Receive path code violation counter 2. |
| Frames Out of Sync Count Register 1 (FOSCR1) | 054h | Receive frame out of sync counter 1 |
| Frames Out of Sync Count Register 2 (FOSCR2) | 055h | Receive frame out of sync counter 2 |
| E-Bit Count Register 1 (E1EBCR1) | 056h | E-bit count register 1. |
| E-Bit Count Register 2 (E1EBCR2) | 057h | E-bit count register 2. |

Note: The addresses shown are for Framer 1. Addresses for Framers 2 to 4 can be calculated using the following: Framer n = (Framer 1 address + $(n - 1) \times 200h$); where $n = 2$ to 4 for Framers 2 to 4.

8.9.7.1 Status and Information Bit Operation

When a particular event has occurred (or is occurring), the appropriate bit in one of these registers is set to 1. Status bits can operate in either a latched or real-time fashion. Some latched bits can be enabled to generate a hardware interrupt via the $\overline{\text{INTB}}$ signal.

8.9.7.1.1 Real-Time Bits

Some status bits operate in a real-time fashion. These bits are read-only and indicate the present state of an alarm or a condition. Real-time bits remain stable and valid during the host read operation. The current value of the internal status signals can be read at any time from the real-time status registers without changing any the latched status register bits.

8.9.7.1.2 Latched Bits

When an event or an alarm occurs and a latched bit is set to 1, it remains set until cleared by the user. These bits typically respond on a change-of-state for an alarm, condition, or event, and operate in a read-then-write fashion. The user should read the value of the desired status bit and then write a 1 to that particular bit location to clear the latched value (write a 0 to locations not to be cleared). Once the bit is cleared, it is not set again until the event has occurred again.

8.9.7.1.3 Mask Bits

Some of the alarms and events can be either masked or unmasked from the interrupt pin via the Receive Interrupt Mask registers ([RIM1:RIM7](#)). When unmasked, the $\overline{\text{INTB}}$ signal is forced low when the enabled event or condition occurs. The $\overline{\text{INTB}}$ pin is allowed to return high (if no other unmasked interrupts are present) when the user reads and then clears (with a write) the alarm bit that caused the interrupt to occur. Note that the latched status bit and the $\overline{\text{INTB}}$ pin clear even if the alarm is still present.

Note that some conditions can have multiple status indications. For example, receive loss of frame (RLOF) provides the following indications:

| | |
|-----------------------------------|--|
| RRTS1.0 (RLOF) | Real-time indication that the receiver is not synchronized with incoming data stream. Read-only bit that remains high as long as the condition is present. |
| RLS1.0 (RLOFD) | Latched indication that the receiver has lost synchronization since the bit was last cleared. Bit clears when written by the user, even if the condition is still present (rising edge detect of RRTS1.0). |
| RLS1.4 (RLOFC) | Latched indication that the receiver has reacquired synchronization since the bit was last cleared. Bit clears when written by the user, even if the condition is still present (falling edge detect of RRTS1.0). |

Table 8-24. T1 Alarm Criteria

| ALARM | | SET CRITERIA | CLEAR CRITERIA |
|---|---|---|---|
| AIS (Blue Alarm) (See Note 1) | | When over a 3ms window, 4 or fewer zeros are received. | When over a 3ms window, 5 or more zeros are received. |
| RAI (Yellow Alarm) | 1) D4 Bit 2 Mode (T1RCR2.0 = 0) | When bit 2 of 256 consecutive channels is set to zero for at least 254 occurrences. | When bit 2 of 256 consecutive channels is set to zero for less than 254 occurrences. |
| | 2) D4 12th F-Bit Mode (T1RCR2.0 = 1) (Note: This mode is also referred to as the "Japanese Yellow Alarm.") | When the 12th framing bit is set to one for two consecutive occurrences. | When the 12th framing bit is set to zero for two consecutive occurrences. |
| | 3) ESF Mode | When 16 consecutive patterns of 00FF appear in the FDL. | When 14 or fewer patterns of 00FF hex out of 16 possible appear in the FDL. |
| LOS (Loss of Signal) (Note: This alarm is also referred to as receive carrier loss (RCL).) | | When 192 consecutive zeros are received. | When 14 or more ones out of 112 possible bit positions are received starting with the first one received. |

Note 1: The definition of the Alarm Indication Signal (Blue Alarm) is an unframed all-ones signal. AIS detectors should be able to operate properly in the presence of a 10E-3 error rate and they should not falsely trigger on a framed all-ones signal. The AIS alarm criteria in the DS26524 has been set to achieve this performance. It is recommended that the RAIS bit be qualified with the RLOF bit.

Note 2: The following terms are equivalent:
 RAIS = Blue Alarm
 RLOS = RCL
 RLOF = Loss of Frame (conventionally RLOS for Dallas Semiconductor devices)
 RRAI = Yellow Alarm

8.9.8 E1 Automatic Alarm Generation

The device can be programmed to automatically transmit AIS or remote alarm. When automatic AIS generation is enabled ([TCR2.6](#) = 1), the device monitors the receive-side framer to determine if any of the following conditions are present: loss of receive frame synchronization, AIS alarm (all ones) reception, or loss of receive carrier (or signal). If any one (or more) of these conditions is present, the framer forces an AIS.

When automatic RAI generation is enabled ([TCR2.5](#) = 1), the framer monitors the receive side to determine if any of the following conditions are present: loss of receive frame synchronization, AIS alarm (all ones) reception, loss of receive carrier (or signal), or if CRC-4 multiframe synchronization cannot be found within 128ms of FAS synchronization (if CRC-4 is enabled). If any one (or more) of the above conditions is present, the framer transmits an RAI alarm. RAI generation conforms to ETS 300 011 and ITU-T G.706 specifications.

Note: It is an illegal state to have both automatic AIS generation and automatic remote alarm generation enabled at the same time.

8.9.8.1 Receive AIS-CI and RAI-CI Detection

AIS-CI is a repetitive pattern of 1.26 seconds. It consists of 1.11 seconds of an unframed all-ones pattern and 0.15 seconds of all ones modified by the AIS-CI signature. The AIS-CI signature is a repetitive pattern 6176 bits in length in which, if the first bit is numbered bit 0, bits 3088, 3474, and 5790 are logical zeros and all other bits in the pattern are logical ones (T1.403). AIS-CI is an unframed pattern, so it is defined for all T1 framing formats. The RAIS-CI bit is set when the AIS-CI pattern has been detected and RAIS ([RRTS1.2](#)) is set. RAIS-CI is a latched bit that should be cleared by the host when read. RAIS-CI continues to set approximately every 1.2 seconds that the condition is present. The host needs to poll the bit in conjunction with the normal AIS indicators to determine when the condition has cleared.

RAI-CI is a repetitive pattern within the ESF data link with a period of 1.08 seconds. It consists of sequentially interleaving 0.99 seconds of “00000000 11111111” (right-to-left) with 90ms of “00111110 11111111.” The RRAI-CI bit is set when a bit-oriented code of “00111110 11111111” is detected while RRAI ([RRTS1.3](#)) is set. The RRAI-CI detector uses the receive BOC filter bits (RBF0 and RBF1) located in RBOCC to determine the integration time for RAI-CI detection. Like RAIS-CI, the RRAI-CI bit is latched and should be cleared by the host when read. RRAI-CI continues to set approximately every 1.1 seconds that the condition is present. The host needs to poll the bit in conjunction with the normal RAI indicators to determine when the condition has cleared. It may be useful to enable the 200ms ESF RAI integration time with the RAIE control bit ([T1RCR2.1](#)) in networks that use RAI-CI.

8.9.8.2 T1 Receive-Side Digital Milliwatt Code Generation

Receive-side digital milliwatt code generation involves using the T1 Receive Digital Milliwatt registers ([T1RDMWE1:T1RDMWE3](#)) to determine which of the 24 T1 channels of the T1 line going to the backplane should be overwritten with a digital milliwatt pattern. The digital milliwatt code is an 8-byte repeating pattern that represents a 1kHz sine wave (1E/0B/0B/1E/9E/8B/8B/9E). Each bit in the [T1RDMWE1](#), [T1RDMWE2](#), and [T1RDMWE3](#) registers represents a particular channel. If a bit is set to 1, the receive data in that channel is replaced with the digital milliwatt code. If a bit is set to 0, no replacement occurs.

8.9.9 Error-Count Registers

The DS26524 contains four counters that are used to accumulate line coding errors, path errors, and synchronization errors. Counter update options include one-second boundaries, 42ms (T1 mode only), 62.5ms (E1 mode only), or manually. See the Error-Counter Configuration register ([ERCNT](#)). When updated automatically, the user can use the interrupt from the timer to determine when to read these registers. All four counters saturate at their respective maximum counts and they will not roll over. (**Note:** Only the Line Code Violation Count register has the potential to overflow, but the bit error would have to exceed 10E-2 before this would occur.)

The DS26524 can share the one-second timer from Port 1 across all ports. All DS26524 error/performance counters can be configured to update on the shared one-second source, or a separate manual update signal input. See the Error-Counter Configuration register [ERCNT](#) register for more information. By allowing multiple framer cores to synchronously latch their counters, the host software can be streamlined to read and process performance information from multiple spans in a more controlled manner.

8.9.9.1 Line Code Violation Count Register (LCVCR)

Either bipolar violations or code violations can be counted. Bipolar violations are defined as consecutive marks of the same polarity. In T1 mode, if the B8ZS mode is set for the receive side, then B8ZS codewords are not counted as BPVs. In E1 mode, if the HDB3 mode is set for the receive side, then HDB3 codewords are not counted as BPVs. If [ERCNT.0](#) is set, then the LCVCR counts code violations as defined in ITU-T O.161. Code violations are defined as consecutive bipolar violations of the same polarity. In most applications, the framer should be programmed to count BPVs when receiving AMI code and to count CVs when receiving B8ZS or HDB3 code. This counter increments at all times and is not disabled by loss of sync conditions. The counter saturates at 65,535 and will not rollover. The bit-error rate on an E1 line would have to be greater than 10E-2 before the PCVCR would saturate. See [Table 8-25](#) and [Table 8-26](#) for details of exactly what the LCVCRs count.

Table 8-25. T1 Line Code Violation Counting Options

| COUNT EXCESSIVE ZEROS? (ERCNT.0) | B8ZS ENABLED? (RCR1.6) | WHAT IS COUNTED IN LCVCR1 , LCVCR2 |
|---|---|---|
| No | No | BPVs |
| Yes | No | BPVs + 16 consecutive zeros |
| No | Yes | BPVs (B8ZS/HDB3 codewords not counted) |
| Yes | Yes | BPVs + 8 consecutive zeros |

Table 8-26. E1 Line Code Violation Counting Options

| E1 CODE VIOLATION SELECT (ERCNT.0) | WHAT IS COUNTED IN LCVCR1 , LCVCR2 |
|---|---|
| 0 | BPVs |
| 1 | CVs |

8.9.9.2 Path Code Violation Count Register (PCVCR)

In T1 operation, the Path Code Violation Count register (PCVCR) records either Ft, Fs, or CRC-6 errors. When the receive side of a framer is set to operate in the T1 ESF framing mode, PCVCR records errors in the CRC-6 codewords. When set to operate in the T1 D4 framing mode, PCVCR counts errors in the Ft framing bit position. Via the [ERCNT.2](#) bit, a framer can be programmed to also report errors in the Fs framing bit position. PCVCR is disabled during receive loss of synchronization (RLOF = 1) conditions. See [Table 8-27](#) for a detailed description of exactly what errors the PCVCR counts in T1 operation.

In E1 operation, PCVCR records CRC-4 errors. Since the maximum CRC-4 count in a one-second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC-4 level; it continues to count if loss of multiframe sync occurs at the CAS level.

The Path Code Violation Count Register 1 ([PCVCR1](#)) is the most significant word and Path Code Violation Count Register 2 ([PCVCR2](#)) is the least significant word of a 16-bit counter that records path violations (PVs).

Table 8-27. T1 Path Code Violation Counting Arrangements

| FRAMING MODE | COUNT Fs ERRORS? | WHAT IS COUNTED IN PCVCR1 , PCVCR2 |
|--------------|------------------|---|
| D4 | No | Errors in the Ft pattern |
| D4 | Yes | Errors in both the Ft and Fs patterns |
| ESF | Don't Care | Errors in the CRC-6 codewords |

8.9.9.3 Frames Out of Sync Count Register (FOSCR)

The FOSCR is used to count the number of multiframes that the receive synchronizer is out of sync. This number is useful in ESF applications needing to measure the parameters loss of frame count (LOFC) and ESF error events as described in AT&T publication TR54016. When the FOSCR is operated in this mode, it is not disabled during receive loss of synchronization (RLOF = 1) conditions. The FOSCR has an alternate operating mode whereby it will count either errors in the Ft framing pattern (in the D4 mode) or errors in the FPS framing pattern (in the ESF mode). When the FOSCR is operated in this mode, it is disabled during receive loss of synchronization (RLOF = 1) conditions. See [Table 8-28](#) for a detailed description of what the FOSCR is capable of counting.

In E1 mode, the FOSCR counts word errors in the frame alignment signal in time slot 0. This counter is disabled when RLOF is high. FAS errors will not be counted when the framer is searching for FAS alignment and/or synchronization at either the CAS or CRC-4 multiframe level. Since the maximum FAS word error count in a one-second period is 4000, this counter cannot saturate.

The Frames Out of Sync Count Register 1 ([FOSCR1](#)) is the most significant word and Frames Out of Sync Count Register 2 ([FOSCR2](#)) is the least significant word of a 16-bit counter that records frames out of sync.

Table 8-28. T1 Frames Out of Sync Counting Arrangements

| FRAMING MODE (RCR1.5) | COUNT MOS OR F-BIT ERRORS (ERCNT.1) | WHAT IS COUNTED IN FOSCR1 , FOSCR2 |
|--|--|---|
| D4 | MOS | Number of multiframes out of sync |
| D4 | F-Bit | Errors in the Ft pattern |
| ESF | MOS | Number of multiframes out of sync |
| ESF | F-Bit | Errors in the FPS pattern |

8.9.9.4 E-Bit Counter (EBCR)

This counter is only available in E1 mode. E-Bit Count Register 1 ([E1EBCR1](#)) is the most significant word and E-Bit Count Register 2 ([E1EBCR2](#)) is the least significant word of a 16-bit counter that records far-end block errors (FEBE) as reported in the first bit of frames 13 and 15 on E1 lines running with CRC-4 multiframe. These count registers increment once each time the received E-bit is set to 0. Since the maximum E-bit count in a one-second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC-4 level; it continues to count if loss of multiframe sync occurs at the CAS level.

8.9.10 DS0 Monitoring Function

The DS26524 can monitor one DS0 (64kbps) channel in the transmit direction and one DS0 channel in the receive direction at the same time. [Table 8-29](#) shows the registers related to the control of transmit and receive DS0.

Table 8-29. Registers Related to DS0 Monitoring

| REGISTER | FRAMER ADDRESSES | FUNCTION |
|---|------------------|-----------------------------------|
| Transmit DS0 Channel Monitor Select (TDS0SEL) | 189h | Transmit channel to be monitored. |
| Transmit DS0 Monitor Register (TDS0M) | 1BBh | Monitored data. |
| Receive Channel Monitor Select Register (RDS0SEL) | 012h | Receive channel to be monitored. |
| Receive DS0 Monitor Register (RDS0M) | 060h | Monitored data. |

Note: The addresses shown are for Framer 1. Addresses for Framers 2 to 4 can be calculated using the following: Framer $n = (\text{Framer 1 address} + (n - 1) \times 200h)$; where $n = 2$ to 4 for Framers 2 to 4.

In the transmit direction, the user determines which channel is to be monitored by properly setting the TCM[4:0] bits in the [TDS0SEL](#) register. In the receive direction, the RCM[4:0] bits in the [RDS0SEL](#) register need to be properly set. The DS0 channel pointed to by the TCM[4:0] bits appear in the Transmit DS0 Monitor register ([TDS0M](#)) and the DS0 channel pointed to by the RCM[4:0] bits appear in the Receive DS0 Monitor register ([RDS0M](#)). The TCM[4:0] and RCM[4:0] bits should be programmed with the decimal decode of the appropriate T1 or E1 channel. T1 channels 1 to 24 map to register values 0 to 23. E1 channels 1 to 32 map to register values 0 to 31. For example, if DS0 channel 6 in the transmit direction and DS0 channel 15 in the receive direction needed to be monitored, then the following values would be programmed into [TDS0SEL](#) and [RDS0SEL](#):

| | |
|----------|----------|
| TCM4 = 0 | RCM4 = 0 |
| TCM3 = 0 | RCM3 = 1 |
| TCM2 = 1 | RCM2 = 1 |
| TCM1 = 0 | RCM1 = 1 |
| TCM0 = 1 | RCM0 = 0 |

8.9.11 Transmit Per-Channel Idle Code Insertion

Channel data can be replaced by an idle code on a per-channel basis in the transmit and receive directions.

The Transmit Idle Code Definition registers ([TIDR1:TIDR32](#)) are provided to set the 8-bit idle code for each channel. The Transmit Channel Idle Code Enable registers ([TCICE1:TCICE4](#)) are used to enable idle code replacement on a per-channel basis.

8.9.12 Receive Per-Channel Idle Code Insertion

Channel data can be replaced by an idle code on a per-channel basis in the transmit and receive directions. The Receive Idle Code Definition registers ([RIDR1:RIDR32](#)) are provided to set the 8-bit idle code for each channel. The Receive Channel Idle Code Enable registers ([RCICE1:RCICE4](#)) are used to enable idle code replacement on a per-channel basis.

8.9.13 Per-Channel Loopback

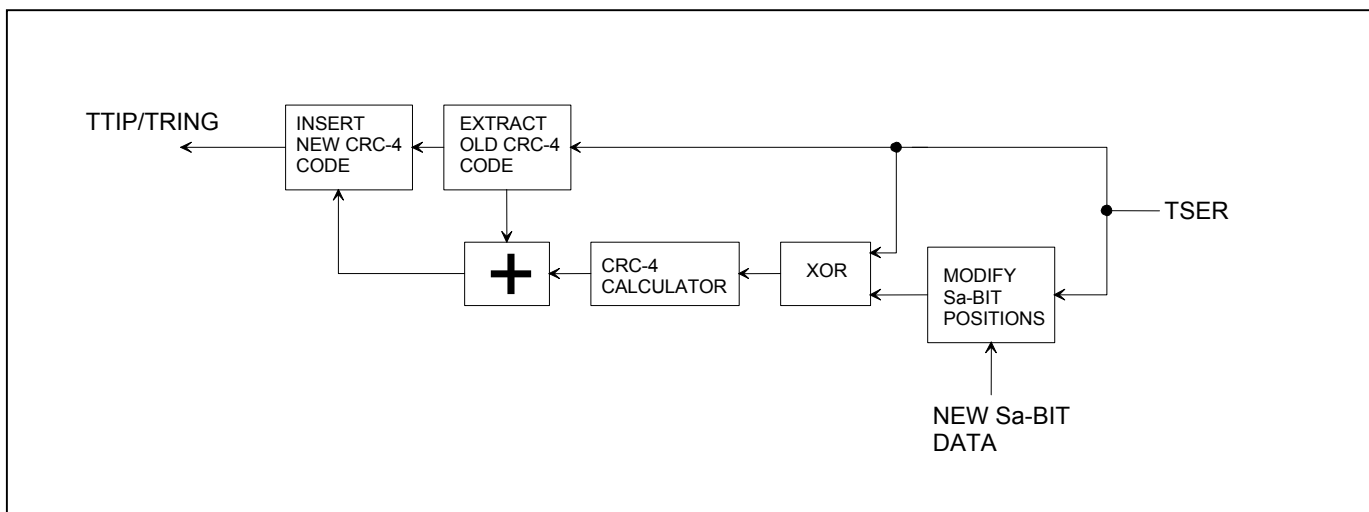
The Per-Channel Loopback Enable registers ([PCL1:PCL4](#)) determine which channels (if any) from the backplane should be replaced with the data from the receive side, i.e., off the T1 or E1 line. If this loopback is enabled, the transmit and receive clocks and frame syncs must be synchronized. One method to accomplish this would be to tie RCLK to TCLK and RFSYNC to TSYNC. There are no restrictions on which channels can be looped back or on how many channels can be looped back.

Each of the bit positions in the Per-Channel Loopback Enable registers ([PCL1:PCL4](#)) represents a DS0 channel in the outgoing frame. When these bits are set to 1, data from the corresponding receive channel replaces the data on [TSER](#) for that channel.

8.9.14 E1 G.706 Intermediate CRC-4 Updating (E1 Mode Only)

The DS26524 can implement the G.706 CRC-4 recalculation at intermediate path points. When this mode is enabled, the data stream presented at TSER will already have the FAS/NFAS, CRC multiframe alignment word, and CRC-4 checksum in time slot 0. The user can modify the Sa-bit positions and this change in data content will be used to modify the CRC-4 checksum. This modification, however, does not corrupt any error information the original CRC-4 checksum may contain. In this mode of operation, TSYNC must be configured to multiframe mode. The data at TSER must be aligned to the TSYNC signal. If TSYNC is an input, the user must assert TSYNC aligned at the beginning of the multiframe relative to TSER. If TSYNC is an output, the user must multiframe align the data presented to TSER. This mode is enabled with the [TCR3.0](#) control bit (CRC4R). Note that the E1 transmitter must already be enabled for CRC insertion with the [TCR1.0](#) control bit (TCRC4).

Figure 8-8. CRC-4 Recalculate Method



8.9.15 T1 Programmable In-Band Loop Code Generator

The DS26524 can generate and detect a repeating bit pattern from one to eight bits or 16 bits in length. **This function is available only in T1 mode.**

Table 8-30. Registers Related to T1 In-Band Loop Code Generator

| REGISTER | FRAMER ADDRESSES | FUNCTION |
|--|------------------|---|
| Transmit Code Definition Register 1 (T1TCD1) | 1ACh | Pattern to be sent for loop code. |
| Transmit Code Definition Register 2 (T1TCD2) | 1ADh | Length of the pattern to be sent. |
| Transmit Control Register 3 (TCR3) | 183h | TLOOP bit for control of number of patterns being sent. |
| Transmit Control Register 4 (TCR4) | 186h | Length of the code being sent. |

Note: The addresses shown are for Framer 1. Addresses for Framers 2 to 4 can be calculated using the following: Framer $n = (\text{Framer 1 address} + (n - 1) \times 200h)$; where $n = 2$ to 4 for Framers 2 to 4.

To transmit a pattern, the user loads the pattern to be sent into the Transmit Code Definition registers ([T1TCD1](#) and [T1TCD2](#)) and selects the proper length of the pattern by setting the TC1 and TC0 bits in Transmit Control Register 4 ([TCR4](#)). When generating a 1-, 2-, 4-, 8-, or 16-bit pattern, both [T1TCD1](#) and [T1TCD2](#) must be filled with the proper code. Generation of a 3-, 5-, 6-, and 7-bit pattern only requires [T1TCD1](#) to be filled. Once this is accomplished, the pattern is transmitted as long as the TLOOP control bit ([TCR3.0](#)) is enabled. Normally (unless the transmit formatter is programmed to not insert the F-bit position) the framer overwrites the repeating pattern once every 193 bits to allow the F-bit position to be sent.

As an example, to transmit the standard loop-up code for Channel Service Units (CSUs), which is a repeating pattern of ...10000100001..., set TCD1 = 80h, TC0 = 0, TC1 = 0, and TCR3.0 = 1.

8.9.16 T1 Programmable In-Band Loop Code Detection

The DS26524 can generate and detect a repeating bit pattern from one to eight bits or 16 bits in length. **This function is available only in T1 mode.**

Table 8-31. Registers Related to T1 In-Band Loop Code Detection

| REGISTER | FRAMER ADDRESSES | FUNCTION |
|--|------------------|--|
| Receive In-Band Code Control Register (T1RIBCC) | 082h | Used for selecting length of receive in-band loop code register. |
| Receive Up Code Definition Register 1 (T1RUPCD1) | 0ACh | Receive up code definition register 1. |
| Receive Up Code Definition Register 2 (T1RUPCD2) | 0ADh | Receive up code definition register 2. |
| Receive Down Code Definition Register 1 (T1RDNCD1) | 0AEh | Receive down code definition register 1. |
| Receive Down Code Definition Register 2 (T1RDNCD2) | 0AFh | Receive up code definition register 2. |
| Receive Spare Code Register 1 (T1RSCD1) | 09Ch | Receive spare code register 1. |
| Receive Spare Code Register 2 (T1RSCD2) | 09Dh | Receive spare code register 2. |
| Receive Real-Time Status Register 3 (RRTS3) | 0B2h | Real-time loop code detect. |
| Receive Latched Status Register 3 (RLS3) | 092h | Latched loop code detect bits. |
| Receive Interrupt Mask Register 3 (RIM3) | 0A2h | Mask for latched loop code detect bits. |

Note: The addresses shown are for Framer 1. Addresses for Framers 2 to 4 can be calculated using the following: Framer n = (Framer 1 address + $(n - 1) \times 200h$); where $n = 2$ to 4 for Framers 2 to 4.

The framer has three programmable pattern detectors. Typically, two of the detectors are used for “loop-up” and “loop-down” code detection. The user programs the codes to be detected in the Receive Up Code Definition registers ([T1RUPCD1](#) and [T1RUPCD2](#)) and the Receive Down Code Definition registers ([T1RDNCD1](#) and [T1RDNCD2](#)). The length of each pattern is selected via the Receive In-Band Code Control register ([T1RIBCC](#)). There is a third detector (Spare) and it is defined and controlled via the [T1RSCD1/T1RSCD2](#) and [T1RSCC](#) registers. When detecting a 16-bit pattern, both receive code definition registers are used together to form a 16-bit register. For 8-bit patterns, both receive code definition registers are filled with the same value. Detection of a 1-, 2-, 3-, 4-, 5-, 6-, and 7-bit pattern only requires the first receive code definition register to be filled. The framer detects repeating pattern codes in both framed and unframed circumstances with bit-error rates as high as $10E-2$. The detectors can handle both F-bit inserted and F-bit overwrite patterns. Writing the least significant byte of the receive code definition register resets the integration period for that detector. The code detector has a nominal integration period of 48ms. Thus, after about 48ms of receiving a valid code, the proper status bit (LUP, LDN, and LSP) is set to 1. Note that real-time status bits, as well as latched set and clear bits, are available for LUP, LDN, and LSP ([RRTS3](#) and [RLS3](#)). Normally codes are sent for a period of 5 seconds. It is recommended that the software poll the framer every 50ms to 100ms until 5 seconds has elapsed to ensure that the code is continuously present.

8.9.17 Framer Payload Loopbacks

The framer, payload, and remote loopbacks are controlled by Receive Control Register 3 ([RCR3](#)).

Table 8-32. Registers Related to Framer Payload Loopbacks

| RECEIVE CONTROL REGISTER 3 (RCR3) | FRAMER ADDRESSES | FUNCTION |
|---|------------------|--|
| Framer Loopback | 083h | Transmit data output from the framer is looped back to the receiver. |
| Payload Loopback | 083h | The 192-bit payload data is looped back to the transmitter. |
| Remote Loopback | 083h | Data recovered by the receiver is looped back to the transmitter. |

Note: The addresses shown are for Framer 1. Addresses for Framers 2 to 4 can be calculated using the following: Framer n = (Framer 1 address + $(n - 1) \times 200h$); where $n = 2$ to 4 for Framers 2 to 4.

8.10 HDLC Controllers

8.10.1 Receive HDLC Controller

The DS26524 has an enhanced HDLC controller that can be mapped into a single time slot, or Sa4 to Sa8 bits (E1 mode), or the FDL (T1 mode). The HDLC controller has a 64-byte FIFO buffer in both the transmit and receive paths. The user can select any specific bits within the time slot(s) to assign to the HDLC controller, as well as specific Sa bits (E1 mode).

The HDLC controller performs all the necessary overhead for generating and receiving performance report messages (PRMs) as described in ANSI T1.403 and the messages as described in AT&T TR54016. The HDLC controller automatically generates and detects flags, generates and checks the CRC check sum, generates and detects abort sequences, stuffs and destuffs zeros, and byte aligns to the data stream. The 64-byte buffers in the HDLC controller are large enough to allow a full PRM to be received or transmitted without host intervention.

[Table 8-33](#) shows the registers related to the HDLC.

Table 8-33. Registers Related to the HDLC

| REGISTER | FRAMER ADDRESSES | FUNCTION |
|---|------------------|---|
| Receive HDLC Control Register (RHC) | 010h | Mapping of the HDLC to DS0 or FDL. |
| Receive HDLC Bit Suppress Register (RHBSE) | 011h | Receive HDLC bit suppression register. |
| Receive HDLC FIFO Control Register (RHFC) | 087h | Determines the length of the receive HDLC FIFO. |
| Receive HDLC Packet Bytes Available Register (RHPBA) | 0B5h | Tells the user how many bytes are available in the receive HDLC FIFO. |
| Receive HDLC FIFO Register (RHF) | 0B6h | The actual FIFO data. |
| Receive Real-Time Status Register 5 (RRTS5) | 0B4h | Indicates the FIFO status. |
| Receive Latched Status Register 5 (RLS5) | 094h | Latched status. |
| Receive Interrupt Mask Register 5 (RIM5) | 0A4h | Interrupt mask for interrupt generation for the latched status. |
| Transmit HDLC Control Register 1 (THC1) | 110h | Miscellaneous transmit HDLC control. |
| Transmit HDLC Bit Suppress Register (THBSE) | 111h | Transmit HDLC bit suppress for bits not to be used. |
| Transmit HDLC Control Register 2 (THC2) | 113h | HDLC to DS0 channel selection and other control. |
| Transmit HDLC FIFO Control Register (THFC) | 187h | Used to control the transmit HDLC FIFO. |
| Transmit Real-Time Status Register 2 (TRTS2) | 1B1h | Indicates the real-time status of the transmit HDLC FIFO. |
| Transmit HDLC Latched Status Register 2 (TLS2) | 191h | Indicates the FIFO status. |
| Transmit Interrupt Mask Register 2 (HDLC) Register (TIM2) | 1A1h | Interrupt mask for the latched status. |
| Transmit HDLC FIFO Buffer Available Register (TFBA) | 1B3h | Indicates the number of bytes that can be written into the transmit FIFO. |
| Transmit HDLC FIFO Register (THF) | 1B4h | Transmit HDLC FIFO. |

Note: The addresses shown are for Framers 1. Addresses for Framers 2 to 4 can be calculated using the following: Framer n = (Framer 1 address + $(n - 1) \times 200h$); where $n = 2$ to 4 for Framers 2 to 4.

8.10.1.1 HDLC FIFO Control

Control of the transmit and receive FIFOs is accomplished via the Receive HDLC FIFO Control ([RHFC](#)) and Transmit HDLC FIFO Control ([THFC](#)) registers. The FIFO control registers set the watermarks for the FIFO.

When the receive FIFO fills above the high watermark, the RHWM bit ([RRTS5.1](#)) is set. RHWM and THRM are real-time bits and remain set as long as the FIFO's write pointer is above the watermark. When the transmit FIFO empties below the low watermark, the TLWM bit in the [TRTS2](#) register is set. TLWM is a real-time bit and remains set as long as the transmit FIFO's write pointer is below the watermark. If enabled, this condition can also cause an interrupt via the INTB pin.

If the receive HDLC FIFO does overrun, the current packet being processed is dropped. The receive FIFO is emptied. The packet status bit in [RRTS5](#) and [RLS5.5](#) (ROVR) indicate an overrun.

8.10.1.2 Receive HDLC Packet Bytes Available

The lower 7 bits of the Receive HDLC Packet Bytes Available register ([RHPBA](#)) indicates the number of bytes (0 to 64) that can be read from the receive FIFO. The value indicated by this register informs the host as to how many bytes can be read from the receive FIFO without going past the end of a message. This value refers to one of four possibilities: the first part of a packet, the continuation of a packet, the last part of a packet, or a complete packet. After reading the number of bytes indicated by this register, the host then checks the HDLC status registers for detailed message status.

If the value in the [RHPBA](#) register refers to the beginning portion of a message or continuation of a message, then the MSB of the RHPBA register returns a value of 1. This indicates that the host can safely read the number of bytes returned by the lower 7 bits of the RHPBA register, but there is no need to check the information register since the packet has not yet terminated (successfully or otherwise).

8.10.1.3 HDLC Status and Information

[RRTS5](#), [RLS5](#), and [TLS2](#) provide status information for the HDLC controller. When a particular event has occurred (or is occurring), the appropriate bit in one of these registers is set to 1. Some of the bits in these registers are latched and some are real-time bits that are not latched. This section contains register descriptions that list which bits are latched and which are real-time. With the latched bits, when an event occurs and a bit is set to 1, it remains set until the user reads and clears that bit. The bit is cleared when a 1 is written to the bit, and it will not be set again until the event has occurred again. The real-time bits report the current instantaneous conditions that are occurring and the history of these bits is not latched.

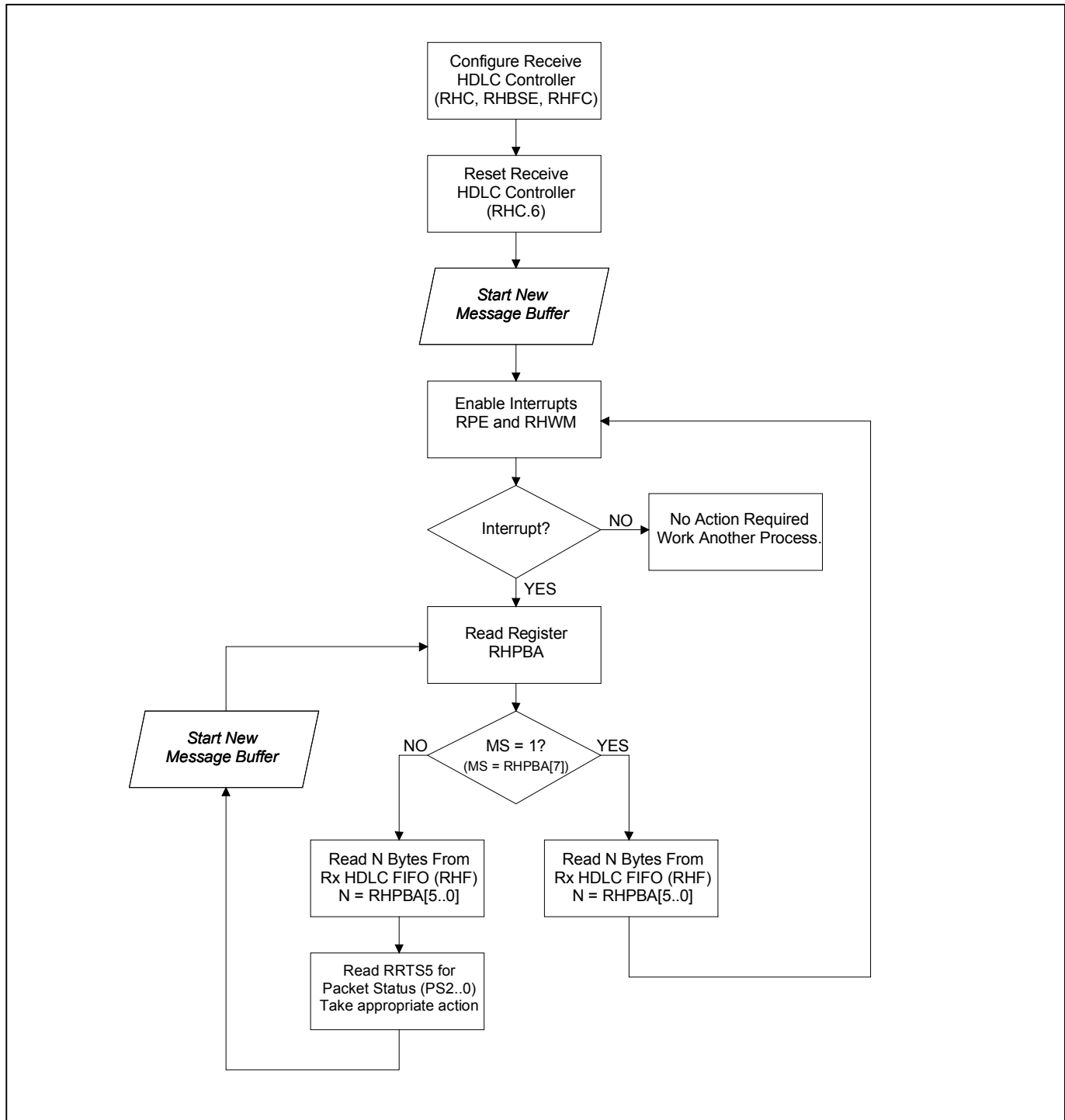
Like the other latched status registers, the user follows a read of the status bit with a write. The byte written to the register informs the device which of the latched bits the user wishes to clear (the real-time bits are not affected by writing to the status register). The user writes a byte to one of these registers, with a 1 in the bit positions he or she wishes to clear and a 0 in the bit positions he or she does not wish to clear.

The HDLC status registers [RLS5](#) and [TLS2](#) have the ability to initiate a hardware interrupt via the $\overline{\text{INTB}}$ output signal. Each of the events in this register can be either masked or unmasked from the interrupt pin via the HDLC interrupt mask registers [RIM5](#) and [TIM2](#). Interrupts force the $\overline{\text{INTB}}$ signal low when the event occurs. The $\overline{\text{INTB}}$ pin is allowed to return high (if no other interrupts are present) when the user reads the event bit that caused the interrupt to occur.

8.10.1.4 HDLC Receive Example

The HDLC status registers in the DS26524 allow for flexible software interface to meet the user's preferences. When receiving HDLC messages, the host can choose to be interrupt driven, or to poll to desired status registers, or a combination of polling and interrupt processes can be used. An example routine for using the DS26524 HDLC receiver is given in [Figure 8-9](#).

Figure 8-9. Receive HDLC Example



8.10.2 Transmit HDLC Controller

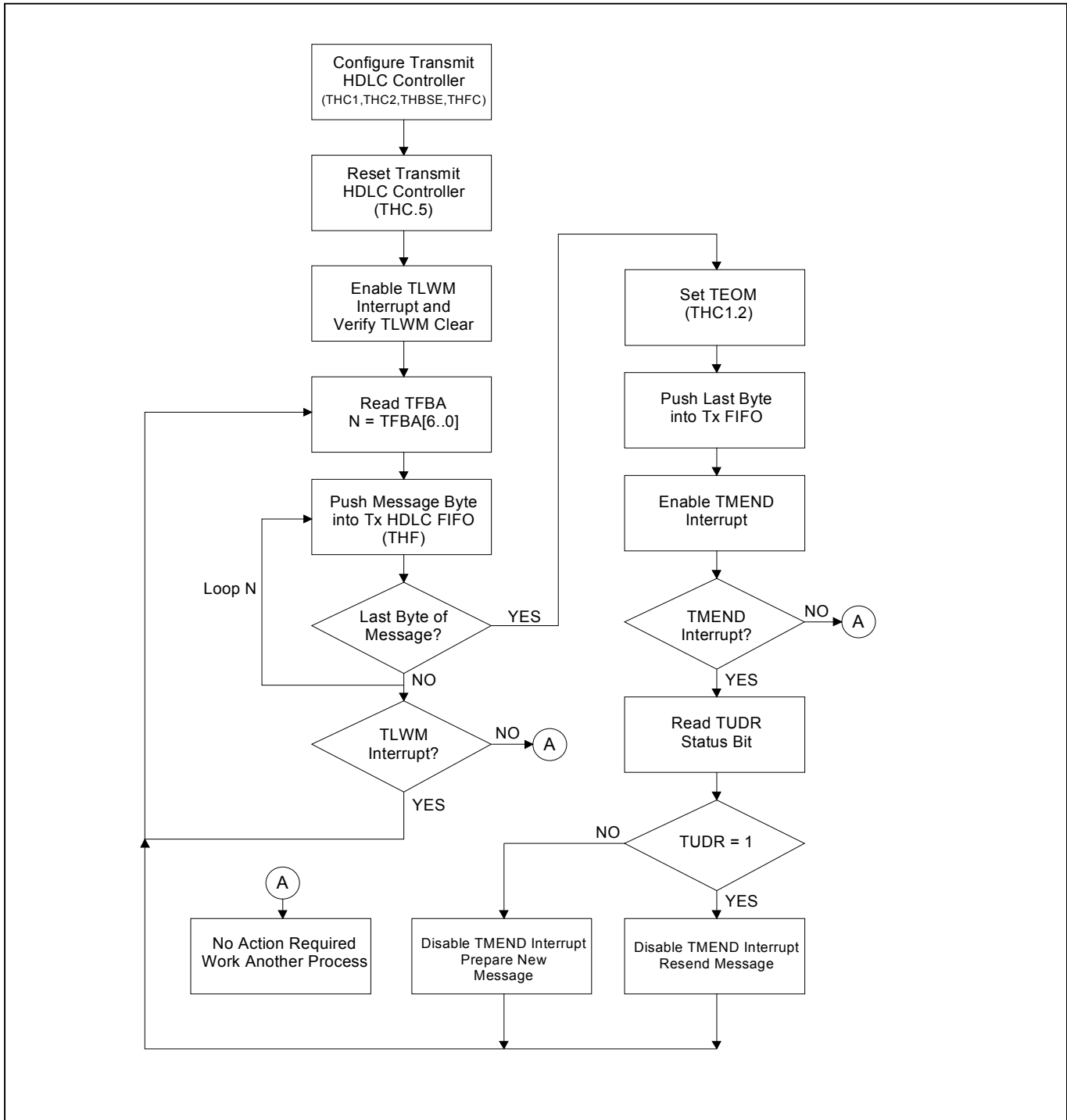
8.10.2.1 FIFO Information

The Transmit HDLC FIFO Buffer Available register ([TFBA](#)) indicates the number of bytes that can be written into the transmit FIFO. The count from this register informs the host as to how many bytes can be written into the transmit FIFO without overflowing the buffer. This is a real-time register. The count shall remain valid and stable during the read cycle.

8.10.2.2 HDLC Transmit Example

The HDLC status registers in the DS26524 allow for flexible software interface to meet the user's preferences. When transmitting HDLC messages, the host can choose to be interrupt driven, or to poll to desired status registers, or a combination of polling and interrupt processes can be used. An example routine for using the DS26524 HDLC receiver is given in [Figure 8-10](#).

Figure 8-10. HDLC Message Transmit Example



8.11 Line Interface Units (LIUs)

The DS26524 has four identical LIU transmit and receive front-ends for the four framers. Each LIU contains three sections: the transmitter, which waveshapes and drives the network line; the receiver, which handles clock and data recovery; and the jitter attenuator. The DS26524 LIUs can switch between T1 or E1 networks without changing any external components on either the transmit or receive side. [Figure 8-11](#) shows a recommended circuit for software-selected termination with protection. In this configuration, the device can connect to 100 Ω T1 twisted pair, 110 Ω J1 twisted pair, 75 Ω or 120 Ω E1 twisted pair without additional component changes. The signals between the framer and LIU are not accessible by the user, thus the framer and LIU cannot be separated. The transmitters have fast high-impedance capability and can be individually powered down.

The DS26524's transmit waveforms meet the corresponding G.703 and T1.102 specifications. Internal software-selectable transmit termination is provided for 100 Ω T1 twisted pair, 110 Ω J1 twisted pair, 120 Ω E1 twisted pair, and 75 Ω E1 coaxial applications. The receiver can connect to 100 Ω T1 twisted pair, 110 Ω J1 twisted pair, 120 Ω E1 twisted pair, and 75 Ω E1 coaxial. The receive LIU can function with a receive signal attenuation of up to 36dB for T1 mode and 43dB for E1 mode. The receiver sensitivity is programmable from 12dB to 43dB of cable loss. Also, a monitor gain setting can be enabled to provide 14dB, 20dB, 26dB, and 32dB of resistive gain.

Figure 8-11. Network Connection for Software-Selected Termination—Longitudinal Protection

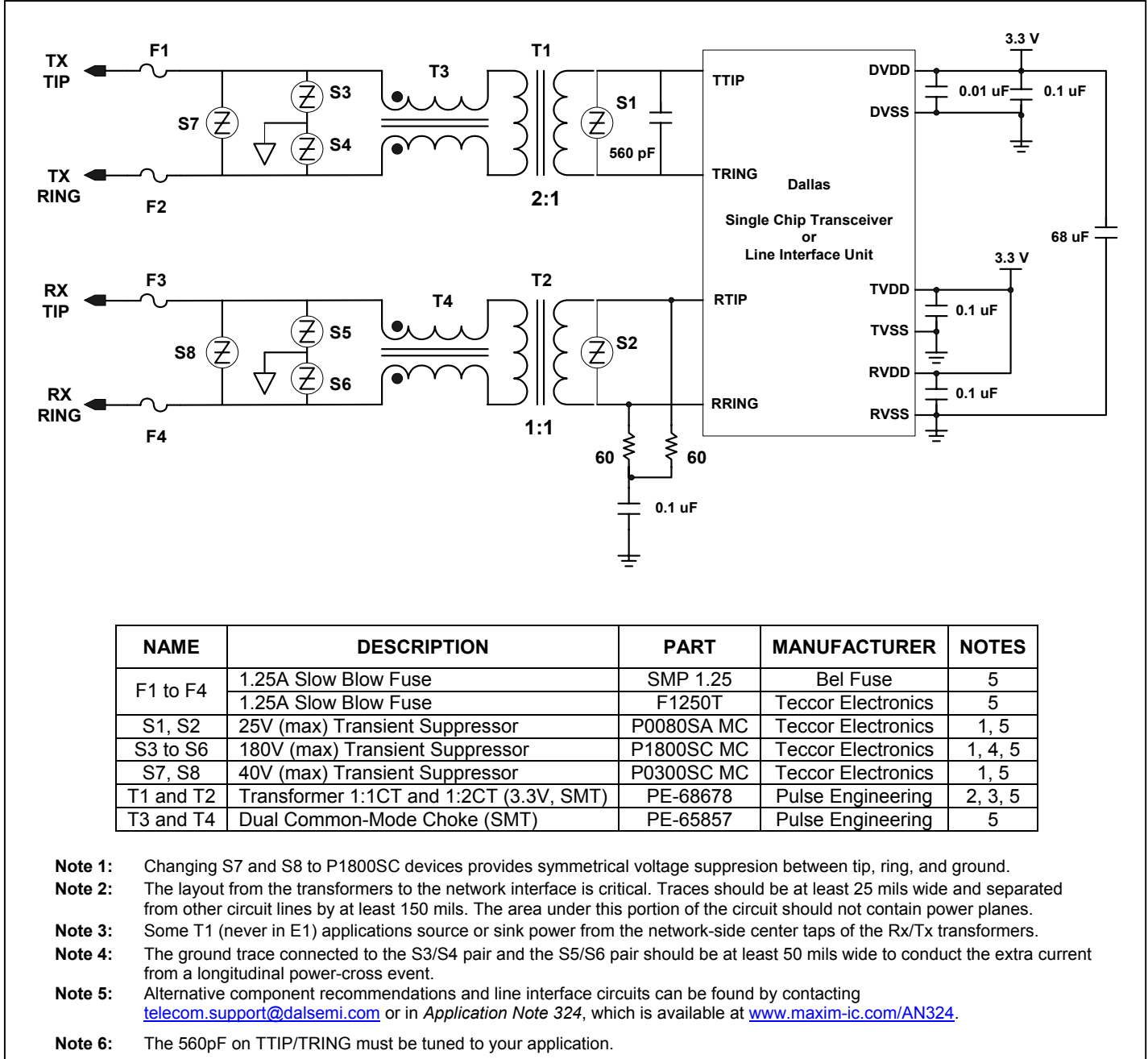


Table 8-34. Recommended Supply Decoupling

| SUPPLY PINS | DECOUPLING CAPACITANCE | NOTES |
|---------------|---|--|
| DVDD/DVSS | $0.01\mu\text{F} + 0.1\mu\text{F} + 1\mu\text{F} + 10\mu\text{F}$ | — |
| DVDDIO/DVSSIO | $0.01\mu\text{F} + 0.1\mu\text{F} + 1\mu\text{F} + 10\mu\text{F}$ | — |
| ATVDD/ATVSS | $0.1\mu\text{F} (\text{x}8) + 1\mu\text{F} (\text{x}4) + 10\mu\text{F} (\text{x}2)$ | It is recommended to use one $0.1\mu\text{F}$ capacitor for each ATVDD/ATVSS pair (8 total), one $1\mu\text{F}$ for every two ATVDD/ATVSS pairs (4 total), and two $10\mu\text{F}$ capacitors for the analog transmit supply pins. These capacitors should be located as close to the intended power pins as possible. |
| ARVDD/ARVSS | $0.1\mu\text{F} (\text{x}8) + 1\mu\text{F} (\text{x}4) + 10\mu\text{F} (\text{x}2)$ | It is recommended to use one $0.1\mu\text{F}$ capacitor for each ARVDD/ARVSS pair (8 total), one $1\mu\text{F}$ for every two ARVDD/ARVSS pairs (4 total), and two $10\mu\text{F}$ capacitors for the analog receive supply pins. These capacitors should be located as close to the intended power pins as possible. |
| ACVDD/ACVSS | $0.1\mu\text{F} + 1\mu\text{F} + 10\mu\text{F}$ | — |

8.11.1 LIU Operation

The analog AMI/HDB3 waveforms off of the E1 lines or the AMI/B8ZS waveform off of the T1 lines are transformer coupled into the RTIP and RRING pins of the DS26524. The user has the option to use internal termination, software selectable for 75Ω/100Ω/110Ω/120Ω applications, or external termination. The LIU recovers clock and data from the analog signal and passes it through the jitter attenuation mux. The DS26524 contains an active filter that reconstructs the analog received signal for the nonlinear losses that occur in transmission. The receive circuitry also is configurable for various monitor applications. The device has a usable receive sensitivity of 0dB to -43dB for E1 and 0dB to -36dB for T1, which allows the device to operate on 0.63mm (22AWG) cables up to 2.5km (E1) and 6k feet (T1) in length. Data input to the transmit side of the LIU is sent via the jitter attenuation mux to the waveshaping circuitry and line driver. The DS26524 drives the E1 or T1 line from the TTIP and TRING pins via a coupling transformer. The line driver can handle both CEPT 30/ISDN-PRI lines for E1 and long-haul (CSU) or short-haul (DSX-1) lines for T1. The registers that control the LIU operation are shown in [Table 8-35](#).

Table 8-35. Registers Related to Control of DS26524 LIU

| REGISTER | FRAMER ADDRESSES | FUNCTION |
|--|------------------|---|
| Global Transceiver Control Register 2 (GTCR2) | 0F2h | Global transceiver control. |
| Global Transceiver Clock Control Register (GTCCR) | 0F3h | MPS selections, backplane clock selections |
| Global LIU Software Reset Register (GLSRR) | 0F5h | Software reset control for the LIU. |
| Global LIU Interrupt Status Register (GLISR) | 0FBh | Interrupt status bit for each of the 4 LIUs. |
| Global LIU Interrupt Mask Register (GLIMR) | 0FEh | Interrupt mask register for the LIU. |
| LIU Transmit Receive Control Register (LTRCR) | 1000h | T1/J1/E1 selection, output tri-state, loss criteria. |
| LIU Transmit Impedance and Pulse Shape Selection Register (LTITSR) | 1001h | Transmit pulse shape and impedance selection. |
| LIU Maintenance Control Register (LMCR) | 1002h | Transmit maintenance and jitter attenuation control register. |
| LIU Real Status Register (LRSR) | 1003h | LIU real-time status register. |
| LIU Status Interrupt Mask Register (LSIMR) | 1004h | LIU mask registers based on latched status bits. |
| LIU Latched Status Register (LLSR) | 1005h | LIU latched status bits related to loss, open circuit, etc. |
| LIU Receive Signal Level Register (LRSL) | 1006h | LIU receive signal level indicator. |
| LIU Receive Impedance and Sensitivity Monitor Register (LRISMR) | 1007h | LIU impedance match and sensitivity monitor. |

Note: The addresses shown are for Framer 1. Addresses for Framers 2 to 4 can be calculated using the following framer: Framer $n = (\text{Framer 1 address} + (n - 1) \times 200h)$; where $n = 2$ to 4 for Framers 2 to 4.

8.11.2 Transmitter

NRZ data arrives from the framer transmitter; the data is encoded with HDB3 or B8ZS or AMI. The encoded data passes through a jitter attenuator if it is enabled for the transmit path. A digital sequencer and DAC are used to generate transmit waveforms compliant with T1.102 and G.703 pulse templates.

A line driver is used to drive an internal matched impedance circuit for provision of 75Ω, 100Ω, 110Ω, and 120Ω terminations. The transmitter couples to the E1 or T1 transmit twisted pair (or coaxial cable in some E1 applications) via a 1:2 step-up transformer. For the device to create the proper waveforms, the transformer used must meet the specifications listed in [Table 8-37](#). The transmitter requires a transmit clock of 2.048MHz for E1 or 1.544MHz for T1/J1 operation.

The DS26524 drivers have a short-circuit and open-circuit detection driver-fail monitor. The TXENABLE pin can high impedance the transmitter outputs for protection switching. The individual transmitters can also be placed in high impedance through register settings. The DS26524 also has functionality for powering down the transmitters individually. The relevant telecommunications specification compliance is shown in [Table 8-36](#).

Table 8-36. Telecommunications Specification Compliance for DS26524 Transmitters

| TRANSMITTER FUNCTION | TELECOMMUNICATIONS COMPLIANCE |
|--|-------------------------------|
| T1 Telecom Pulse Template Compliance | ANSI T1.403 |
| T1 Telecom Pulse Template Compliance | ANSI T1.102 |
| Transmit Electrical Characteristics for E1 Transmission and Return Loss Compliance | ITU-T G.703 |

Table 8-37. Transformer Specifications

| SPECIFICATION | | RECOMMENDED VALUE |
|------------------------------------|-----------------------|--------------------------------------|
| Turns Ratio 3.3V Applications | | 1:1 (receive) and 1:2 (transmit) ±2% |
| Primary Inductance | | 600μH minimum |
| Leakage Inductance | | 1.0μH maximum |
| Intertwining Capacitance | | 40pF maximum |
| Transmit Transformer DC Resistance | Primary (Device Side) | 1.0Ω maximum |
| | Secondary | 2.0Ω maximum |
| Receive Transformer DC Resistance | Primary (Device Side) | 1.2Ω maximum |
| | Secondary | 1.2Ω maximum |

8.11.2.1 Transmit-Line Pulse Shapes

The DS26524 transmitters can be selected individually to meet the pulse templates for E1 and T1/J1 modes. The T1/J1 pulse template is shown in [Figure 8-12](#). The E1 pulse template is shown in [Figure 8-13](#). The transmit pulse shape can be configured for each LIU on an individual basis. The LIU transmit impedance selection registers can be used to select an internal transmit terminating impedance of 100Ω for T1, 110Ω for J1 mode, 75Ω or 120Ω for E1 mode or no internal termination for E1 or T1 mode. The transmit pulse shape and terminating impedance is selected by [LTITSR](#) registers. The pulse shapes will be compliant to T1.102 and G.703. Pulse shapes are measured for compliance at the appropriate network interface (NI). For T1 long haul and E1, the pulse shape is measured at the far end. For T1 short haul, the pulse shape is measured at the near end.

Figure 8-12. T1/J1 Transmit Pulse Templates

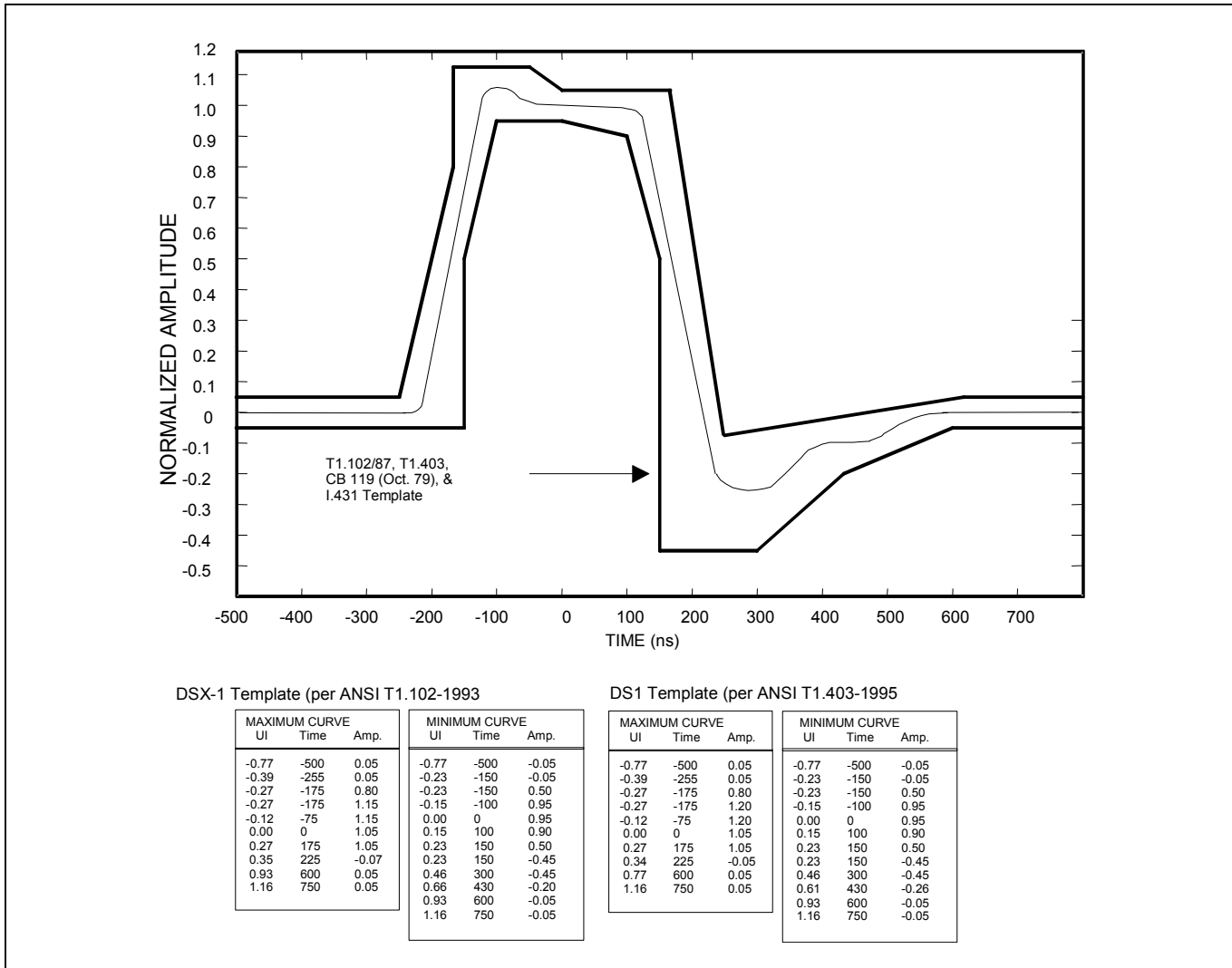
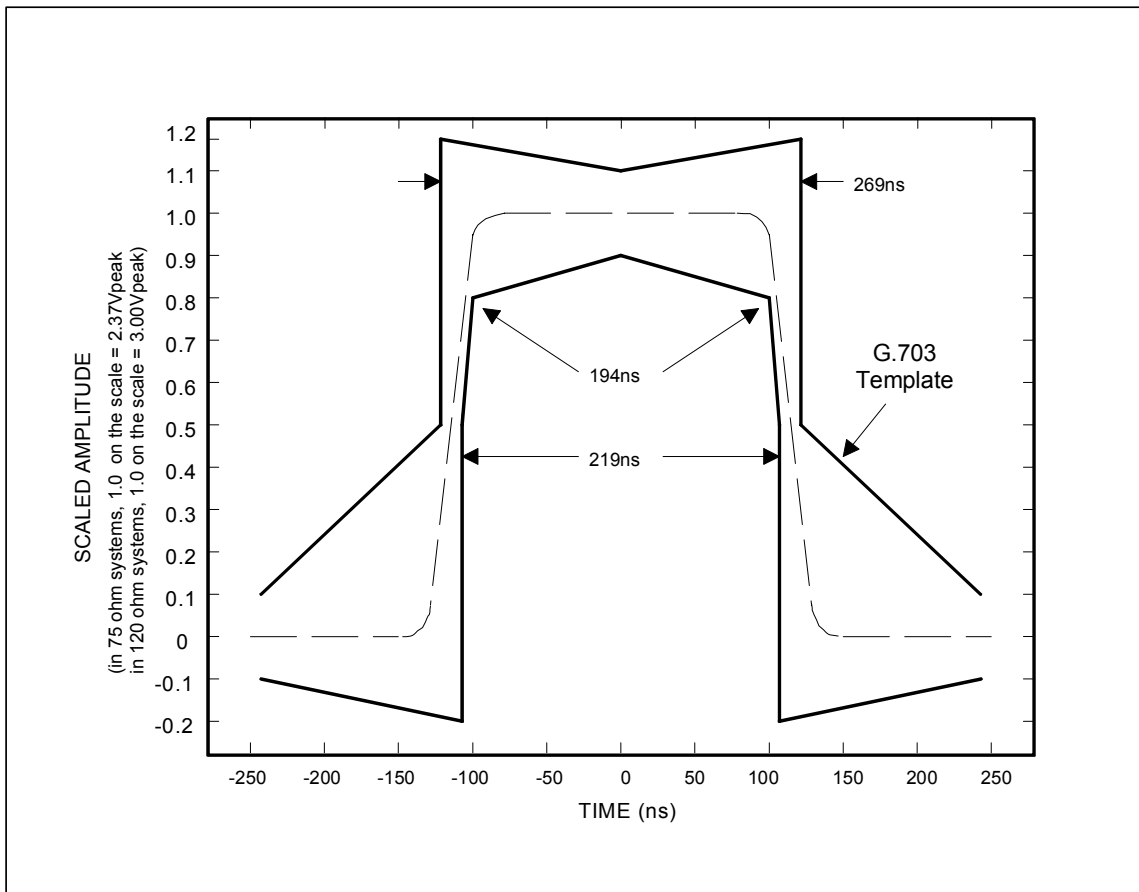


Figure 8-13. E1 Transmit Pulse Templates

8.11.2.2 Transmit Power-Down

The individual transmitters can be powered down by setting the TPDE bit in the LIU Maintenance Control register ([LMCR](#)). Note that powering down the transmit LIU results in a high-impedance state for the corresponding TTIP and TRING pins.

When transmit all ones (AIS) is invoked, continuous ones are transmitted using MCLK as the timing reference. Data input from the framer is ignored. AIS can be sent by setting a bit in the [LMCR](#). Transmit all ones will also be sent if the corresponding receiver goes into LOS state and the ATAIS bit is set in the [LMCR](#).

8.11.2.3 Transmit Short-Circuit Detector/Limiter

Each transmitter has an automatic short-circuit current limiter that activates when the load resistance is approximately 25Ω or less. SCS ([LRSR.2](#)) provides a real-time indication of when the current limiter is activated. The LIU Latched Status register ([LLSR](#)) provides latched versions of the information, which can be used to activate an interrupt when enabled via the [LSIMR](#) register.

8.11.2.4 Transmit Open-Circuit Detector

The DS26524 can also detect when the TTIP or TRING outputs are open circuited. OCS ([LRSR.1](#)) provides a real-time indication of when an open circuit is detected. Register [LLSR](#) provides latched versions of the information, which can be used to activate an interrupt when enabled via the [LSIMR](#) register. The open-circuit detect feature is not available in T1 CSU operating modes (LBO5, LBO6, and LBO7).

8.11.3 Receiver

The DS26524 contains four identical receivers. The four receivers are designed to be fully software-selectable for E1, T1, and J1 without the need to change any external resistors. The device couples to the receive E1 or T1 twisted pair (or coaxial cable in 75Ω E1 applications) via a 1:1 or 2:1 transformer. See [Table 8-37](#) for transformer details. Receive termination and sensitivity are user configurable. Receive termination is configurable for 75Ω, 100Ω, 110Ω, or 120Ω termination by setting the appropriate RIMPM[1:0] bits ([LRISMR](#)). When using the internal termination feature, the resistors labeled Rr in [Figure 8-11](#) should be 60Ω each. If external termination is required, the resistors need to be 37.5Ω, 50Ω, or 60Ω each depending on the line impedance. Receive sensitivity is configurable by setting the appropriate RSMS[1:0] bits ([LRISMR](#)).

The DS26524 uses a digital clock recovery system. The resultant E1, T1, or J1 clock derived from MCLK is multiplied by 16 via an internal PLL and fed to the clock recovery system. The clock recovery system uses the clock from the PLL circuit to form a 16 times oversampler, which is used to recover the clock and data. This oversampling technique offers outstanding performance to meet jitter tolerance specifications shown in [Figure 8-15](#).

Normally, the clock that is output at the RCLK pin is the recovered clock from the E1 AMI/HDB3 or T1 AMI/B8ZS waveform presented at the RTIP and RRING inputs. If the jitter attenuator ([LTRCR](#)) is placed in the receive path (as is the case in most applications), the jitter attenuator restores the RCLK to an approximate 50% duty cycle. If the jitter attenuator is either placed in the transmit path or is disabled, the RCLK output can exhibit slightly shorter high cycles of the clock. This is due to the highly oversampled digital clock recovery circuitry. See [Table 12-2](#) for more details. When no signal is present at RTIP and RRING, a receive carrier loss (RCL) condition occurs and the RCLK is derived from the JACLK source.

8.11.3.1 Receive Level Indicator

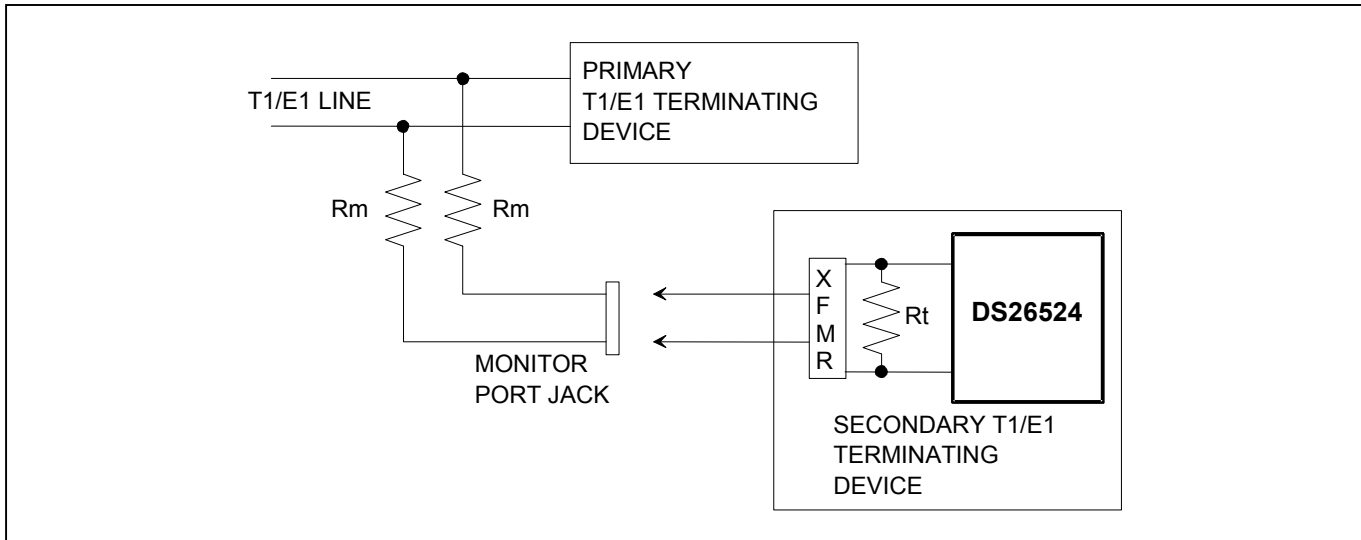
The DS26524 reports the signal strength at RTIP and RRING in approximately 2.5dB increments via RSL[3:0] located in the LIU Receive Signal Level register ([LRSL](#)). This feature is helpful when trouble shooting line performance problems.

8.11.3.2 Receive G.703 Section 10 Synchronization Signal

The DS26524 can receive a 2.048MHz square-wave synchronization clock as specified in Section 10 of ITU-T G.703. To use this mode, set the receive G.703 clock-enable bit RG703 ([LRISMR.7](#)) found in the LIU Receive Impedance and Sensitivity Monitor register ([LRISMR](#)).

8.11.3.3 Receiver Monitor Mode

The receive equalizer is equipped with a monitor mode function that is used to overcome the signal attenuation caused by the resistive bridge used in monitoring applications. This function allows for a resistive gain of up to 32dB, along with cable attenuation of 12dB to 30dB as shown in the LIU Receive Impedance and Sensitivity Monitor register ([LRISMR](#)).

Figure 8-14. Typical Monitor Application**8.11.3.4 Loss of Signal (LOS)**

The DS26524 uses both the digital and analog loss-detection method in compliance with the latest ANSI T1.231 for T1/J1 and ITU-T G.775, or ETS 300 233 for E1 mode of operation.

Loss of signal (LOS) is detected if the receiver level falls below a threshold analog voltage for certain duration. Alternatively, this can be termed as having received “0s” for a certain duration. The signal level and timing duration are defined in accordance with the ANSI T1.231, ITU-T G.775, or ETS 300 233 specifications.

For short-haul mode, the loss-detection thresholds are based on cable loss of 12dB to 18dB for both T1/J1 and E1 modes. The loss thresholds are selectable based on [Table 9-19](#). For long-haul mode, the LOS detection threshold is based on cable loss of 30dB to 38dB for T1/J1 and 30dB to 45dB for E1 mode. Note there is no explicit bit called short-haul mode selection. Loss declaration level is set at 3dB lower than the maximum sensitivity setting programmed in [Table 9-19](#).

The loss state is exited when the receiver detects a certain ones density at the maximum sensitivity level or higher, which is 3dB higher than the loss-detection level. The loss-detection signal level and loss-reset signal level are defined with hysteresis to prevent the receiver from bouncing between “LOS” and “no LOS” states. [Table 8-38](#) outlines the specifications governing the loss function.

Table 8-38. ANSI T1.231, ITU-T G.775, and ETS 300 233 Loss Criteria Specifications

| CRITERIA | STANDARD | | |
|----------------|---|--|---|
| | ANSI T1.231 | ITU-T G.775 | ETS 300 233 |
| Loss Detection | No pulses are detected for 175 ± 75 bits. | No pulses are detected for duration of 10 to 255-bit periods. | No pulses are detected for a duration of 2048-bit periods or 1ms. |
| Loss Reset | Loss is terminated if a duration of 12.5% ones are detected over duration of 175 ± 75 bits. Loss is not terminated if 8 consecutive zeros are found if B8ZS encoding is used. If B8ZS is not used, loss is not terminated if 100 consecutive pulses are zero. | The incoming signal has transitions for duration of 10 to 255-bit periods. | Loss reset criteria are not defined. |

8.11.3.5 ANSI T1.231 for T1 and J1 Modes

For short-haul mode, loss is declared if the received signal level is 3dB lower from the programmed value (based on [Table 9-19](#)) for a duration of 192-bit periods. Hence, if the sensitivity is programmed to be 12dB, loss will be declared at 15dB. LOS is reset if the following criteria are met:

- 1) 24 or more ones are detected in 192-bit period with a programmed sensitivity level measured at RTIP and RRING.
- 2) During the 192 bits, fewer than 100 consecutive zeros are detected.

For long-haul mode, loss is detected if the received signal level is 3dB lower from the programmed value (based on [Table 9-19](#)) for a duration of 192-bit periods. Hence, if the sensitivity is programmed at 30dB, loss declaration level will be 33dB. LOS is reset if the following criteria are met:

- 1) 24 or more ones are detected in 192-bit period with a programmed sensitivity level measured at RTIP and RRING.
- 2) During the 192 bits, fewer than 100 consecutive zeros are detected.

8.11.3.6 ITU-T G.775 for E1 Modes

For short-haul mode, loss is declared if the received signal level is 3dB lower from the programmed value (based on [Table 9-19](#)) for a duration of 192-bit periods. Hence, if the sensitivity is programmed to be 12dB, loss will be declared at 15dB. LOS is reset if the receive signal level is greater than or equal to the programmed sensitivity level for a duration of 192-bit periods.

For long-haul mode, loss is detected if the received signal level is 3dB lower from the programmed value (based on [Table 9-19](#)) for a duration of 192-bit periods. Hence, if the sensitivity is programmed at 30dB, loss declaration level will be 33dB. LOS is reset if the receive signal level is greater than or equal to the programmed sensitivity level for a duration of 192-bit periods.

8.11.3.7 ETS 200 233 for E1 Modes

For short-haul mode, loss is declared if the received signal level is 3dB lower from the programmed value (based on [Table 9-19](#)) continuous duration of 2048-bit periods (1ms). LOS is reset if the receive signal level is greater than or equal to programmed sensitivity level for a duration of 192-bit periods.

For long-haul mode, loss is declared if the received signal level is 3dB lower from the programmed value (based on [Table 9-19](#)) continuous duration of 2048-bit periods (1ms). LOS is reset if the receive signal level is greater than or equal to the programmed sensitivity level for a duration of 192-bit periods.

8.11.4 Jitter Attenuator

The DS26524 contains a jitter attenuator for each LIU that can be set to a depth of 32 or 128 bits via the JADS ([LTRCR.4](#)) bit in the LIU Transmit Receive Control register ([LTRCR](#)).

The 128-bit mode is used in applications where large excursions of wander are expected. The 32-bit mode is used in delay-sensitive applications. The characteristics of the attenuation are shown in [Figure 8-15](#). The jitter attenuator can be placed in either the receive path, the transmit path, or disabled by appropriately setting the JAPS1 and JAPS0 bits in [LTRCR](#).

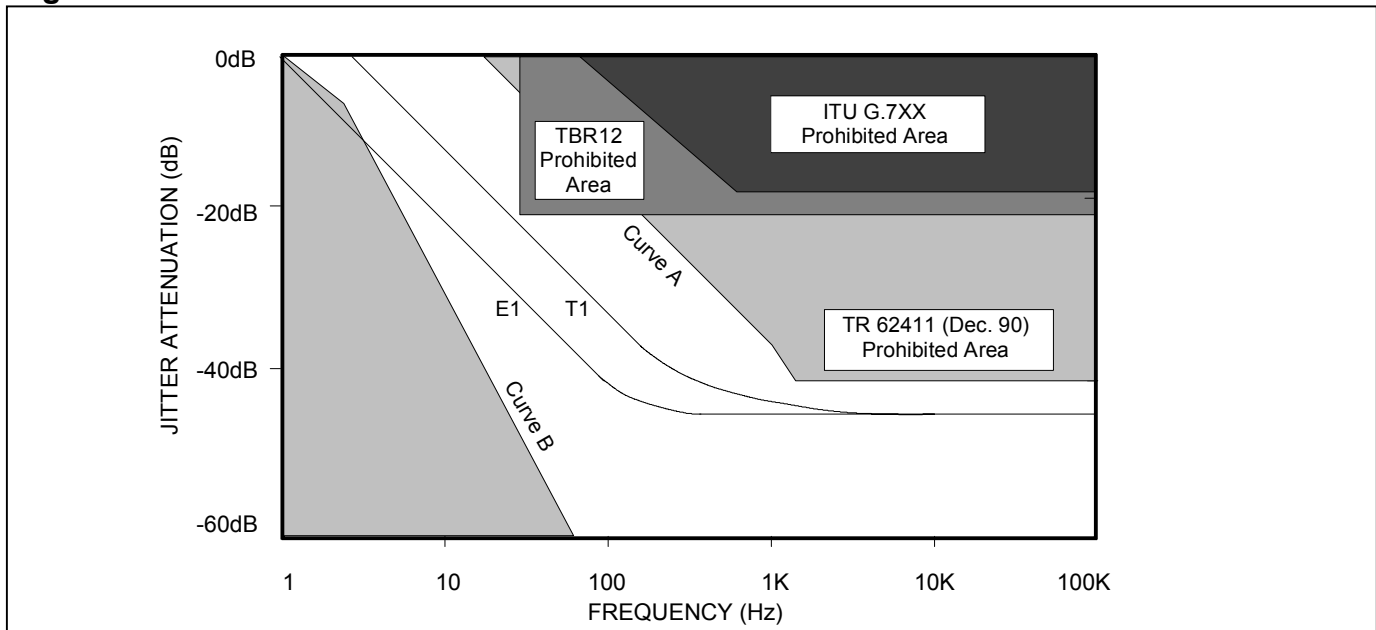
For the jitter attenuator to operate properly, a 2.048MHz, 1.544MHz, or a multiple of up to 8x clock must be applied at MCLK. See the Global Transceiver Clock Control register ([GTCCR](#)) for MCLK options. ITU-T specification G.703 requires an accuracy of ± 50 ppm for both T1/J1 and E1 applications. TR62411 and ANSI specs require an accuracy of ± 32 ppm for T1/J1 interfaces. Circuitry adjusts either the recovered clock from the clock/data recovery block or the clock applied at the TCLK pin to create a smooth jitter-free clock, which is used to clock data out of the jitter attenuator FIFO. It is acceptable to provide a gapped/bursty clock at the TCLK pin if the jitter attenuator is placed in the transmit side. If the incoming jitter exceeds either 120UI_{P-P} (buffer depth is 128 bits) or 28UI_{P-P} (buffer depth is 32 bits), the DS26524 sets the jitter attenuator limit trip set (JALTS) bit in the LIU Latched Status register ([LLSR.3](#)). In T1/J1 mode, the jitter attenuator corner frequency is 3.75Hz and in E1 mode it is 0.6Hz.

The DS26524 jitter attenuator is compliant with the following specifications shown in [Table 8-39](#).

Table 8-39. Jitter Attenuator Standards Compliance

| STANDARD |
|------------------------------------|
| ITU-T I.431, G.703, G.736, G.823 |
| ETS 300 011, TBR 12/13 |
| AT&T TR62411, TR43802 |
| TR-TSY-009, TR-TSY-253, TR-TSY-499 |

Figure 8-15. Jitter Attenuation



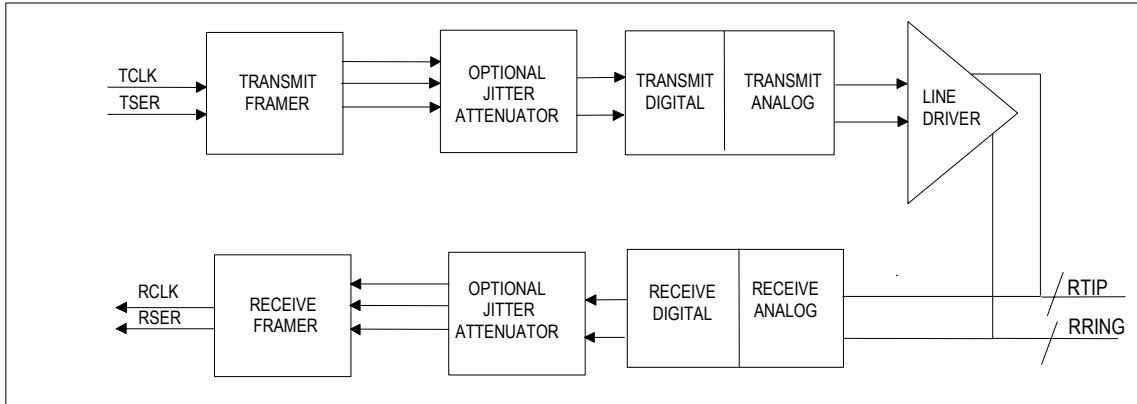
8.11.5 LIU Loopbacks

The DS26524 provides four LIU loopbacks for diagnostic purposes: analog loopback, local loopback, remote loopback, and dual loopback. In the loopback diagrams that follow, TSER, TCLK, RSER, and RCLK are inputs/outputs from the framer. Note that the framer input/output can be in IBO mode where a single TSER/RSER can be shared by up to eight framers.

8.11.5.1 Analog Loopback

The analog output of the transmitter TTIP and TRING is looped back to RTIP and RRING of the receiver. Data at RTIP and RRING is ignored in analog loopback. This is shown in [Figure 8-16](#).

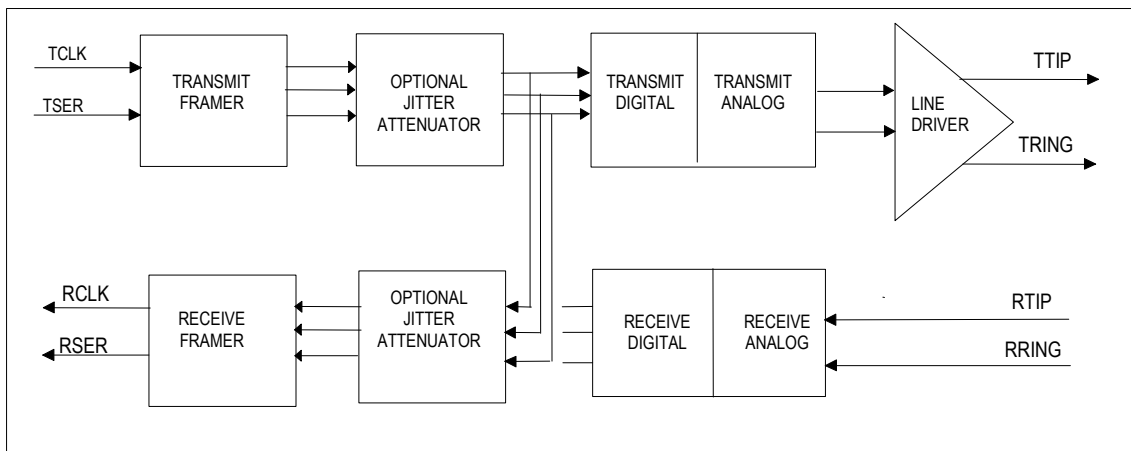
Figure 8-16. Analog Loopback



8.11.5.2 Local Loopback

The transmit system data (the internal signals TPOS, TNEG, and TCLK) is looped back to receive-side inputs to the receive jitter attenuator. The data is also output on TTIP and TRING. Signals at RTIP and RRING are ignored. This loopback is conceptually shown in [Figure 8-17](#).

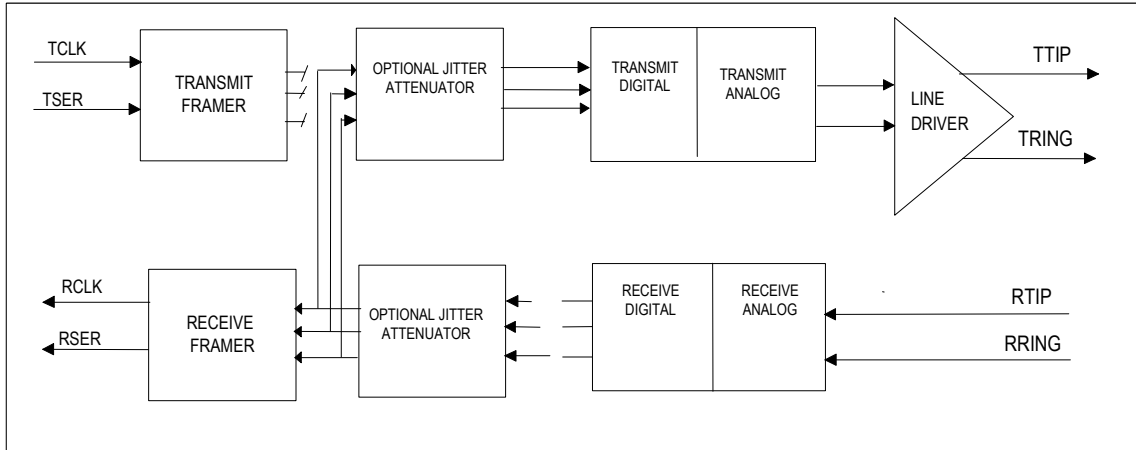
Figure 8-17. Local Loopback



8.11.5.3 Remote Loopback

The outputs decoded from the receive LIU are looped back to the transmit LIU. The inputs from the transmit framer are ignored during a remote loopback. This loopback is conceptually shown in [Figure 8-18](#).

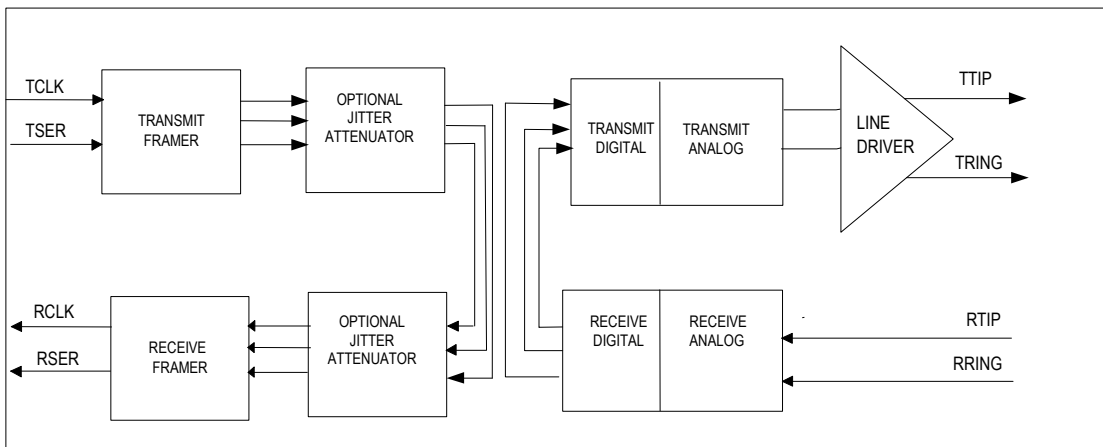
Figure 8-18. Remote Loopback



8.11.5.4 Dual Loopback

The inputs decoded from the receive LIU are looped back to the transmit LIU. The inputs from the transmit framer are looped back to the receiver with the optional jitter attenuator. This loopback is invoked if RLB and LLB are both set in the LIU Maintenance Control register ([LMCR](#)). This loopback is conceptually shown in [Figure 8-19](#).

Figure 8-19. Dual Loopback



8.12 Bit-Error-Rate Test (BERT) Function

The bit-error-rate tester (BERT) block can generate and detect both pseudorandom and repeating bit patterns. It is used to test and stress data-communication links. BERT functionality is dedicated for each of the transceivers. [Table 8-40](#) shows the registers related to the configure, control, and status of the BERT.

Table 8-40. Registers Related to BERT Configure, Control, and Status

| REGISTER | FRAMER ADDRESSES | FUNCTION |
|--|------------------------|--|
| Global BERT Interrupt Status Register (GBISR) | 0FAh | When any of the four BERTs issue an interrupt, a bit is set. |
| Global BERT Interrupt Mask Register (GBIMR) | 0FDh | When any of the four BERTs issue an interrupt, a bit is set. |
| Receive Expansion Port Control Register (RXPC) | 08Ah | Enable for the receiver BERT. |
| Receive BERT Port Bit Suppress Register (RBPBS) | 08Bh | Bit suppression for the receive BERT. |
| Receive BERT Port Channel Select Registers 1 to 4 (RBPCS1 : RBPCS4) | 0D4h, 0D5h, 0D6h, 0D7h | Channels to be enabled for the framer to accept data from the BERT pattern generator. |
| Transmit Expansion Port Control Register (TXPC) | 18Ah | Enable for the transmitter BERT |
| Transmit BERT Port Bit Suppress Register (TBPBS) | 18Bh | Bit suppression for the transmit BERT |
| Transmit BERT Port Channel Select Registers 1 to 4 (TBPCS1 : TBPCS4) | 1D4h, 1D5h, 1D6h, 1D7h | Channels to be enabled for the framer to accept data from the transmit BERT pattern generator. |
| BERT Alternating Word Count Rate Register (BAWC) | 1100h | BERT alternating pattern count register. |
| BERT Repetitive Pattern Set Register 1 (BRP1) | 1101h | BERT repetitive pattern set register 1. |
| BERT Repetitive Pattern Set Register 2 (BRP2) | 1102h | BERT repetitive pattern set register 2. |
| BERT Repetitive Pattern Set Register 3 (BRP3) | 1103h | BERT repetitive pattern set register 3. |
| BERT Repetitive Pattern Set Register 4 (BRP4) | 1104h | BERT repetitive pattern set register 4. |
| BERT Control Register 1 (BC1) | 1105h | Pattern selection and miscellaneous control. |
| BERT Control Register 2 (BC2) | 1106h | BERT bit pattern length control. |
| BERT Bit Count Register 1 (BBC1) | 1107h | BERT bit counter—increments for BERT bit clocks. |
| BERT Bit Count Register 2 (BBC2) | 1108h | BERT bit counter. |
| BERT Bit Count Register 3 (BBC3) | 1109h | BERT bit counter. |
| BERT Bit Count Register 4 (BBC4) | 110Ah | BERT bit counter. |
| BERT Error Count Register 1 (BEC1) | 110Bh | BERT error counter. |
| BERT Error Count Register 2 (BEC2) | 110Ch | BERT error counter. |
| BERT Error Count Register 3 (BEC3) | 110Dh | BERT error counter. |
| BERT Latched Status Register (BLSR) | 110Eh | BERT status registers—denotes synchronization loss and other status. |
| BERT Status Interrupt Mask Register (BSIM) | 110Fh | BERT Interrupt mask. |

Note: The addresses shown are for Framer 1. Addresses for Framers 2 to 4 can be calculated using the following framer: Framer $n = (\text{Framer 1 address} + (n - 1) \times 200\text{h})$; where $n = 2$ to 4 for Framers 2 to 4.

The BERT block can generate and detect the following patterns:

- The pseudorandom patterns 2E7-1, 2E9-1, 2E11-1, 2E15-1, and QRSS
- A repetitive pattern from 1 to 32 bits in length
- Alternating (16-bit) words that flip every 1 to 256 words
- Daly pattern

The BERT function must be enabled and configured in the [TXPC](#) and [RXPC](#) registers for each port. The BERT can then be assigned on a per-channel basis for both the transmitter and receiver, using the special per-channel function in the [TBPCS1:TBPCS4](#) and [RBCS1:RBCS4](#) registers. Individual bit positions within the channels can be suppressed with the [TBPBS](#) and [RBPBS](#) registers. Using combinations of these functions, the BERT pattern can be transmitted and/or received in single or across multiple DS0s, contiguous or broken. Transmit and receive bandwidth assignments are independent of each other.

The BERT receiver has a 32-bit bit counter and a 24-bit error counter. The BERT receiver can generate interrupts on: a change in receive-synchronizer status, receive all zeros, receive all ones, error counter overflow, bit counter overflow, and bit error detection. Interrupts from each of these events can be masked within the BERT function via the BERT Status Interrupt Mask register ([BSIM](#)). If the software detects that the BERT has reported an event, then the software must read the BERT Latched Status register ([BLSR](#)) to determine which event(s) has occurred.

8.12.1 BERT Repetitive Pattern Set

These registers must be properly loaded for the BERT to generate and synchronize to a repetitive pattern, a pseudorandom pattern, alternating word pattern, or a Daly pattern. For a repetitive pattern that is fewer than 32 bits, the pattern should be repeated so that all 32 bits are used to describe the pattern. For example, if the pattern was the repeating 5-bit pattern ...01101... (where the rightmost bit is the one sent first and received first), then BRP1 should be loaded with ADh, BRP2 with B5h, BRP3 with D6h, and BRP4 should be loaded with 5Ah. For a pseudorandom pattern, all four registers should be loaded with all ones (i.e., FFh). For an alternating word pattern, one word should be placed into BRP1 and BRP2 and the other word should be placed into BRP3 and BRP4. For example, if the DDS stress pattern "7E" is to be described, the user would place 00h in BRP1, 00h in BRP2, 7Eh in BRP3, and 7Eh in BRP4, and the alternating word counter would be set to 50 (decimal) to allow 100 bytes of 00h followed by 100 bytes of 7Eh to be sent and received.

8.12.2 BERT Error Counter

Once the BERT has achieved synchronization, this 24-bit counter will increment for each data bit received in error. Toggling the LC control bit in BC1 can clear this counter. This counter saturates when full and will set the BECO status bit in the [BLSR](#) register.

9. DEVICE REGISTERS

Thirteen address bits are used to control the settings of the registers. The address map is compatible with the Dallas Semiconductor octal framer product, DS26528 and DS26401.

The registers control functions of the framers, LIU, and BERT within the DS26524. The map is divided into four framers, followed by four LIUs and four BERTs. Global registers (applicable to all four transceivers and BERTs) are located within the address space of Framer 1.

The bulk write mode is a special mode to write all four transceivers with one write command (see the [GTCR1](#) register). [Figure 9-1](#) shows the register map.

The register details are provided in the following tables. The framer registers bits are provided for Framer 0, and address bits A[11:8] determine the framer addressed.

9.1 Register Listings

Table 9-1. Register Address Ranges (in Hex)

| CHANNEL | GLOBAL REGISTERS | RECEIVE FRAMER | TRANSMIT FRAMER | LIU | BERT |
|---------|------------------|----------------|-----------------|-----------|-----------|
| — | 00F0–00FF | — | — | — | — |
| CH1 | — | 0000–00EF | 0100–01EF | 1000–101F | 1100–110F |
| CH2 | — | 0200–02EF | 0300–03EF | 1020–103F | 1110–111F |
| CH3 | — | 0400–04EF | 0500–05EF | 1040–105F | 1120–112F |
| CH4 | — | 0600–06EF | 0700–07EF | 1060–107F | 1130–113F |

Figure 9-1. Register Memory Map for the DS26524

| | | |
|--|---------------------------|-------------------|
| Adrs = 0000 0000 0000 | Framer 1 Rx Regs 240 Regs | 000 |
| Adrs = 0000 1111 0000 | Global Registers | 0EF 0F0 |
| Adrs = 0001 0000 0000 | Framer 1 Tx Regs 240 Regs | 0FF 100 |
| Adrs = 0001 1111 0000 | Reserved | 1EF 1F0 1FF |
| Adrs = 0010 0000 0000 | Framer 2 Regs | 200 |
| Adrs = 0100 0000 0000 | Framer 3 Regs | 3FF 400 |
| Adrs = 0101 1111 1111 Adrs = 0110 0000 0000 | Framer 4 Regs | 5FF 600 |
| Adrs = 0111 1111 1111 Adrs = 1000 0000 0000 | Reserved | 7FF 800 |
| Adrs = 01111 1111 1111 Adrs = 10000 0000 0000 | LIU Regs | FFF 1000 |
| Adrs = 10000 1111 1111 Adrs = 10001 0000 0000 | BERT | 10FF 1100 |
| Adrs = 10001 0111 1111 | Reserved | 117F |
| Adrs = 11111 1111 1111 | Reserved | 1FFF |

9.1.1 Global Register List

Table 9-2. Global Register List

| GLOBAL REGISTER LIST | | | |
|----------------------|-----------------------|--|-----|
| ADDRESS | NAME | DESCRIPTION | R/W |
| 0F0h | GTCR1 | Global Transceiver Control Register 1 | R/W |
| 0F1h | GFCR | Global Framer Control Register | R/W |
| 0F2h | GTCR2 | Global Transceiver Control Register 2 | R/W |
| 0F3h | GTCCR | Global Transceiver Clock Control Register | R/W |
| 0F4h | — | Reserved | — |
| 0F5h | GLSRR | Global LIU Software Reset Register | R/W |
| 0F6h | GFSRR | Global Framer and BERT Software Reset Register | R/W |
| 0F7h | — | Reserved | — |
| 0F8h | IDR | Device Identification Register | R |
| 0F9h | GFISR | Global Framer Interrupt Status Register | R |
| 0FAh | GBISR | Global BERT Interrupt Status Register | R |
| 0FBh | GLISR | Global LIU Interrupt Status Register | R |
| 0FCh | GFIMR | Global Framer Interrupt Mask Register | R/W |
| 0FDh | GBIMR | Global BERT Interrupt Mask Register | R/W |
| 0FEh | GLIMR | Global LIU Interrupt Mask Register | R/W |
| 01Fh | — | Reserved | — |

Note 1: Reserved registers should only be written with all zeros.

Note 2: The global registers are located in the framer address space. The corresponding address space for the other framers is "Reserved," and should be initialized with all zeros for proper operation.

9.1.2 Framer Register List

Table 9-3. Framer Register List

Note: Only the Framer 1 address is presented here. The same set of register definitions applies for transceiver 2 to 4 in accordance with the DS26524 map offsets. Transceiver offset is $(n - 1) \times 200$ hex, where n designates the transceiver in question.

| FRAMER REGISTER LIST | | | |
|----------------------|--------------------------|--|-----|
| ADDRESS | NAME | DESCRIPTION | R/W |
| 000h–00Fh | — | Reserved | — |
| 010h | RHC | Receive HDLC Control Register | R/W |
| 011h | RHBSE | Receive HDLC Bit Suppress Register | R/W |
| 012h | RDS0SEL | Receive Channel Monitor Select Register | R/W |
| 013h | RSIGC | Receive-Signaling Control Register | R/W |
| 014h | T1RCR2 | Receive Control Register 2 (T1 Mode) | R/W |
| | E1RSAIMR | Receive Sa-Bit Interrupt Mask Register (E1 Mode) | |
| 015h | T1RBOCC | Receive BOC Control Register (T1 Mode Only) | R/W |
| 016h–01Fh | — | Reserved | — |
| 020h | RIDR1 | Receive Idle Code Definition Register 1 | R/W |
| 021h | RIDR2 | Receive Idle Code Definition Register 2 | R/W |
| 022h | RIDR3 | Receive Idle Code Definition Register 3 | R/W |
| 023h | RIDR4 | Receive Idle Code Definition Register 4 | R/W |
| 024h | RIDR5 | Receive Idle Code Definition Register 5 | R/W |
| 025h | RIDR6 | Receive Idle Code Definition Register 6 | R/W |
| 026h | RIDR7 | Receive Idle Code Definition Register 7 | R/W |
| 027h | RIDR8 | Receive Idle Code Definition Register 8 | R/W |
| 028h | RIDR9 | Receive Idle Code Definition Register 9 | R/W |
| 029h | RIDR10 | Receive Idle Code Definition Register 10 | R/W |
| 02Ah | RIDR11 | Receive Idle Code Definition Register 11 | R/W |
| 02Bh | RIDR12 | Receive Idle Code Definition Register 12 | R/W |
| 02Ch | RIDR13 | Receive Idle Code Definition Register 13 | R/W |
| 02Dh | RIDR14 | Receive Idle Code Definition Register 14 | R/W |
| 02Eh | RIDR15 | Receive Idle Code Definition Register 15 | R/W |
| 02Fh | RIDR16 | Receive Idle Code Definition Register 16 | R/W |
| 030h | RIDR17 | Receive Idle Code Definition Register 17 | R/W |
| 031h | RIDR18 | Receive Idle Code Definition Register 18 | R/W |
| 032h | RIDR19 | Receive Idle Code Definition Register 19 | R/W |
| 033h | RIDR20 | Receive Idle Code Definition Register 20 | R/W |
| 034h | RIDR21 | Receive Idle Code Definition Register 21 | R/W |
| 035h | RIDR22 | Receive Idle Code Definition Register 22 | R/W |
| 036h | RIDR23 | Receive Idle Code Definition Register 23 | R/W |
| 037h | RIDR24 | Receive Idle Code Definition Register 24 | R/W |
| 038h | T1RSAOI1 | Receive-Signaling All-Ones Insertion Register 1 (T1 Mode Only) | R/W |
| | RIDR25 | Receive Idle Code Definition Register 25 (E1 Mode) | |
| 039h | T1RSAOI2 | Receive-Signaling All-Ones Insertion Register 2 (T1 Mode Only) | R/W |
| | RIDR26 | Receive Idle Code Definition Register 26 (E1 Mode) | |
| 03Ah | T1RSAOI3 | Receive-Signaling All-Ones Insertion Register 3 (T1 Mode Only) | R/W |
| | RIDR27 | Receive Idle Code Definition Register 27 (E1 Mode) | |
| 03B | RIDR28 | Receive Idle Code Definition Register 28 (E1 Mode) | — |
| 03C | T1RDMWE1 | T1 Receive Digital Milliwatt Enable Register 1 (T1 Mode Only) | R/W |
| | RIDR29 | Receive Idle Code Definition Register 29 (E1 Mode) | |
| 03Dh | T1RDMWE2 | T1 Receive Digital Milliwatt Enable Register 2 (T1 Mode Only) | R/W |
| | RIDR30 | Receive Idle Code Definition Register 30 (E1 Mode) | |
| 03Eh | T1RDMWE3 | T1 Receive Digital Milliwatt Enable Register 3 (T1 Mode Only) | R/W |
| | RIDR31 | Receive Idle Code Definition Register 31 (E1 Mode) | |

| FRAMER REGISTER LIST | | | |
|----------------------|--------------------------|--|-----|
| ADDRESS | NAME | DESCRIPTION | R/W |
| 03Fh | RIDR32 | Receive Idle Code Definition Register 32 (E1 Mode) | — |
| 040h | RS1 | Receive-Signaling Register 1 | R |
| 041h | RS2 | Receive-Signaling Register 2 | R |
| 042h | RS3 | Receive-Signaling Register 3 | R |
| 043h | RS4 | Receive-Signaling Register 4 | R |
| 044h | RS5 | Receive-Signaling Register 5 | R |
| 045h | RS6 | Receive-Signaling Register 6 | R |
| 046h | RS7 | Receive-Signaling Register 7 | R |
| 047h | RS8 | Receive-Signaling Register 8 | R |
| 048h | RS9 | Receive-Signaling Register 9 | R |
| 049h | RS10 | Receive-Signaling Register 10 | R |
| 04Ah | RS11 | Receive-Signaling Register 11 | R |
| 04Bh | RS12 | Receive-Signaling Register 12 | R |
| 04Ch | RS13 | Receive-Signaling Register 13 (E1 Mode only) | — |
| 04Dh | RS14 | Receive-Signaling Register 14 (E1 Mode only) | — |
| 04Eh | RS15 | Receive-Signaling Register 15 (E1 Mode only) | — |
| 04Fh | RS16 | Receive-Signaling Register 16 (E1 Mode only) | — |
| 050h | LCVCR1 | Line Code Violation Count Register 1 | R |
| 051h | LCVCR2 | Line Code Violation Count Register 2 | R |
| 052h | PCVCR1 | Path Code Violation Count Register 1 | R |
| 053h | PCVCR2 | Path Code Violation Count Register 2 | R |
| 054h | FOSCR1 | Frames Out of Sync Count Register 1 | R |
| 055h | FOSCR2 | Frames Out of Sync Count Register 2 | R |
| 056h | E1EBCR1 | E-Bit Counter 1 (E1 Mode Only) | R |
| 057h | E1EBCR2 | E-Bit Counter 2 (E1 Mode Only) | R |
| 058h–05Fh | — | Reserved | — |
| 060 | RDS0M | Receive DS0 Monitor Register | R |
| 061 | — | Reserved | — |
| 062h | T1RFDL | Receive FDL Register (T1 Mode) | R |
| | E1RRTS7 | Receive Real-Time Status Register 7 (E1 Mode) | |
| 063h | T1RBOC | Receive BOC Register (T1 Mode) | R |
| 064h | T1RSLC1 | Receive SLC-96 Data Link Register 1 (T1 Mode) | R |
| | E1RAF | E1 Receive Align Frame Register (E1 Mode) | |
| 065h | T1RSLC2 | Receive SLC-96 Data Link Register 2 (T1 Mode) | R |
| | E1RNAF | E1 Receive Non-Align Frame Register (E1 Mode) | |
| 066h | T1RSLC3 | Receive SLC-96 Data Link Register 3 (T1 Mode) | R |
| | E1RSiAF | E1 Received Si Bits of the Align Frame Register (E1 Mode) | |
| 067h | E1RSiNAF | Received Si Bits of the Non-Align Frame Register (E1 Mode) | R |
| 068h | E1RRA | Received Remote Alarm Register (E1 Mode) | R |
| 069h | E1RSa4 | E1 Receive Sa4 Bits Register (E1 Mode Only) | R |
| 06Ah | E1RSa5 | E1 Receive Sa5 Bits Register (E1 Mode Only) | R |
| 06Bh | E1RSa6 | E1 Receive Sa6 Bits Register (E1 Mode Only) | R |
| 06Ch | E1RSa7 | E1 Receive Sa7 Bits Register (E1 Mode Only) | R |
| 06Dh | E1RSa8 | Receive Sa8 Bits Register (E1 Mode Only) | R |
| 06Eh | SaBITS | E1 Receive SaX Bits Register | R |
| 06Fh | Sa6CODE | Received Sa6 Codeword Register | R |
| 070h–07Fh | — | Reserved | — |
| 080h | RMMR | Receive Master Mode Register | R/W |
| 081h | RCR1 | Receive Control Register 1 (T1 Mode) | R/W |
| | RCR1 | Receive Control Register 1 (E1 Mode) | |
| 082h | T1RIBCC | Receive In-Band Code Control Register (T1 Mode) | R/W |
| | E1RCR2 | Receive Control Register 2 (E1 Mode) | |

| FRAMER REGISTER LIST | | | |
|----------------------|--------------------------|--|-----|
| ADDRESS | NAME | DESCRIPTION | R/W |
| 083h | RCR3 | Receive Control Register 3 | R/W |
| 084h | RIOCR | Receive I/O Configuration Register | R/W |
| 085h | RESCR | Receive Elastic Store Control Register | R/W |
| 086h | ERCNT | Error-Counter Configuration Register | R/W |
| 087h | RHFC | Receive HDLC FIFO Control Register | R/W |
| 088h | RIBOC | Receive Interleave Bus Operation Control Register | R/W |
| 089h | T1RSCC | In-Band Receive Spare Control Register (T1 Mode Only) | R/W |
| 08Ah | RXPC | Receive Expansion Port Control Register | R/W |
| 08B | RBPBS | Receive BERT Port Bit Suppress Register | R/W |
| 08Ch–08Fh | — | Reserved | — |
| 090h | RLS1 | Receive Latched Status Register 1 | R/W |
| 091h | RLS2 | Receive Latched Status Register 2 | R/W |
| 092h | RLS3 | Receive Latched Status Register 3 | R/W |
| 093 | RLS4 | Receive Latched Status Register 4 | R/W |
| 094h | RLS5 | Receive Latched Status Register 5 (HDLC) | R/W |
| 095h | — | Reserved | — |
| 096h | RLS7 | Receive Latched Status Register 7 (T1 Mode) | R/W |
| | RLS7 | Receive Latched Status Register 7 (E1 Mode) | |
| 097h | — | Reserved | — |
| 098h | RSS1 | Receive-Signaling Status Register 1 | R/W |
| 099h | RSS2 | Receive-Signaling Status Register 2 | R/W |
| 09Ah | RSS3 | Receive-Signaling Status Register 3 | R/W |
| 09Bh | RSS4 | Receive-Signaling Status Register 4 (E1 Mode Only) | R/W |
| 09Ch | T1RSCD1 | Receive Spare Code Definition Register 1 (T1 Mode Only) | R/W |
| 09Dh | T1RSCD2 | Receive Spare Code Definition Register 2 (T1 Mode Only) | R/W |
| 09Eh | — | Reserved | — |
| 09Fh | RIIR | Receive Interrupt Information Register | R/W |
| 0A0h | RIM1 | Receive Interrupt Mask Register 1 | R/W |
| 0A1h | RIM2 | Receive Interrupt Mask Register 2 (E1 Mode Only) | R/W |
| 0A2h | RIM3 | Receive Interrupt Mask Register 3 (T1 Mode) | R/W |
| | RIM3 | Receive Interrupt Mask Register 3 (E1 Mode) | |
| 0A3h | RIM4 | Receive Interrupt Mask Register 4 | R/W |
| 0A4h | RIM5 | Receive Interrupt Mask Register 5 (HDLC) | R/W |
| 0A5h | — | Reserved | — |
| 0A6h | RIM7 | Receive Interrupt Mask Register 7 (T1 Mode) | R/W |
| 0A7h | — | Reserved | — |
| 0A8h | RSCSE1 | Receive-Signaling Change of State Enable Register 1 | R/W |
| 0A9h | RSCSE2 | Receive-Signaling Change of State Enable Register 2 | R/W |
| 0AAh | RSCSE3 | Receive-Signaling Change of State Enable Register 3 | R/W |
| 0ABh | RSCSE4 | Receive-Signaling Change of State Enable Register 4 (E1 Mode Only) | — |
| 0ACh | T1RUPCD1 | Receive Up Code Definition Register 1 (T1 Mode Only) | R/W |
| 0ADh | T1RUPCD2 | Receive Up Code Definition Register 2 (T1 Mode Only) | R/W |
| 0AEh | T1RDNCD1 | Receive Down Code Definition Register 1 (T1 Mode Only) | R/W |
| 0AFh | T1RDNCD2 | Receive Down Code Definition Register 2 (T1 Mode Only) | R/W |
| 0B0h | RRTS1 | Receive Real-Time Status Register 1 | R |
| 0B1h | — | Reserved | — |
| 0B2h | RRTS3 | Receive Real-Time Status Register 3 (T1 Mode) | R |
| | RRTS3 | Receive Real-Time Status Register 3 (E1 Mode) | |
| 0B3h | — | Reserved | — |
| 0B4h | RRTS5 | Receive Real-Time Status Register 5 (HDLC) | R |
| 0B5h | RHPBA | Receive HDLC Packet Bytes Available Register | R |
| 0B6h | RHF | Receive HDLC FIFO Register | R |

| FRAMER REGISTER LIST | | | |
|----------------------|--------------------------------|---|-----|
| ADDRESS | NAME | DESCRIPTION | R/W |
| 0B7h–0BFh | — | Reserved | — |
| 0C0h | RBCS1 | Receive Blank Channel Select Register 1 | R/W |
| 0C1h | RBCS2 | Receive Blank Channel Select Register 2 | R/W |
| 0C2h | RBCS3 | Receive Blank Channel Select Register 3 | R/W |
| 0C3h | RBCS4 | Receive Blank Channel Select Register 4 (E1 Mode Only) | R/W |
| 0C4h | RCBR1 | Receive Channel Blocking Register 1 | R/W |
| 0C5h | RCBR2 | Receive Channel Blocking Register 2 | R/W |
| 0C6h | RCBR3 | Receive Channel Blocking Register 3 | R/W |
| 0C7h | RCBR4 | Receive Channel Blocking Register 4 (E1 Mode Only) | R/W |
| 0C8h | RSI1 | Receive-Signaling Reinsertion Enable Register 1 | R/W |
| 0C9h | RSI2 | Receive-Signaling Reinsertion Enable Register 2 | R/W |
| 0CAh | RSI3 | Receive-Signaling Reinsertion Enable Register 3 | R/W |
| 0CBh | RSI4 | Receive-Signaling Reinsertion Enable Register 4 (E1 Mode Only) | R/W |
| 0CCh | RGCCS1 | Receive Gapped Clock Channel Select Register 1 | R/W |
| 0CDh | RGCCS2 | Receive Gapped Clock Channel Select Register 2 | R/W |
| 0CEh | RGCCS3 | Receive Gapped Clock Channel Select Register 3 | R/W |
| 0CFh | RGCCS4 | Receive Gapped Clock Channel Select Register (E1 Mode Only) | R/W |
| 0D0h | RCICE1 | Receive Channel Idle Code Enable Register 1 | R/W |
| 0D1h | RCICE2 | Receive Channel Idle Code Enable Register 2 | R/W |
| 0D2h | RCICE3 | Receive Channel Idle Code Enable Register 3 | R/W |
| 0D3h | RCICE4 | Receive Channel Idle Code Enable Register 4 (E1 Mode Only) | R/W |
| 0D4h | RBPCS1 | Receive BERT Port Channel Select Register 1 | R/W |
| 0D5h | RBPCS2 | Receive BERT Port Channel Select Register 2 | R/W |
| 0D6h | RBPCS3 | Receive BERT Port Channel Select Register 3 | R/W |
| 0D7h | RBPCS4 | Receive BERT Port Channel Select Register (E1 Mode Only) | R/W |
| 0D8h–0EFh | — | Reserved | — |
| 0F0h–0FFh | Global Registers (Section 9.3) | See the Global Register list in Table 9-2 . Note that this space is “Reserved” in Framers 2 to 4. | R/W |
| 100h–10Fh | — | Reserved | — |
| 110h | THC1 | Transmit HDLC Control Register 1 | R/W |
| 111h | THBSE | Transmit HDLC Bit Suppress Register | R/W |
| 112h | — | Reserved | — |
| 113h | THC2 | Transmit HDLC Control Register 2 | R/W |
| 114h | E1TSACR | E1 Transmit Sa-Bit Control Register (E1 Mode) | R/W |
| 115h–117h | — | Reserved | — |
| 118h | SSIE1 | Software-Signaling Insertion Enable Register 1 | R/W |
| 119h | SSIE2 | Software-Signaling Insertion Enable Register 2 | R/W |
| 11Ah | SSIE3 | Software-Signaling Insertion Enable Register 3 | R/W |
| 11Bh | SSIE4 | Software-Signaling Insertion Enable Register 4 (E1 Mode Only) | R/W |
| 11Ch–11Fh | — | Reserved | — |
| 120h | TIDR1 | Transmit Idle Code Definition Register 1 | R/W |
| 121h | TIDR2 | Transmit Idle Code Definition Register 2 | R/W |
| 122h | TIDR3 | Transmit Idle Code Definition Register 3 | R/W |
| 123h | TIDR4 | Transmit Idle Code Definition Register 4 | R/W |
| 124h | TIDR5 | Transmit Idle Code Definition Register 5 | R/W |
| 125h | TIDR6 | Transmit Idle Code Definition Register 6 | R/W |
| 126h | TIDR7 | Transmit Idle Code Definition Register 7 | R/W |
| 127h | TIDR8 | Transmit Idle Code Definition Register 8 | R/W |
| 128h | TIDR9 | Transmit Idle Code Definition Register 9 | R/W |
| 129h | TIDR10 | Transmit Idle Code Definition Register 10 | R/W |
| 12Ah | TIDR11 | Transmit Idle Code Definition Register 11 | R/W |

| FRAMER REGISTER LIST | | | |
|----------------------|--------------------------|---|-----|
| ADDRESS | NAME | DESCRIPTION | R/W |
| 12Bh | TIDR12 | Transmit Idle Code Definition Register 12 | R/W |
| 12Ch | TIDR13 | Transmit Idle Code Definition Register 13 | R/W |
| 12Dh | TIDR14 | Transmit Idle Code Definition Register 14 | R/W |
| 12Eh | TIDR15 | Transmit Idle Code Definition Register 15 | R/W |
| 12Fh | TIDR16 | Transmit Idle Code Definition Register 16 | R/W |
| 130h | TIDR17 | Transmit Idle Code Definition Register 17 | R/W |
| 131h | TIDR18 | Transmit Idle Code Definition Register 18 | R/W |
| 132h | TIDR19 | Transmit Idle Code Definition Register 19 | R/W |
| 133h | TIDR20 | Transmit Idle Code Definition Register 20 | R/W |
| 134h | TIDR21 | Transmit Idle Code Definition Register 21 | R/W |
| 135h | TIDR22 | Transmit Idle Code Definition Register 22 | R/W |
| 136h | TIDR23 | Transmit Idle Code Definition Register 23 | R/W |
| 137h | TIDR24 | Transmit Idle Code Definition Register 24 | R/W |
| 138h | TIDR25 | Transmit Idle Code Definition Register 25 (E1 Mode Only) | R/W |
| 139h | TIDR26 | Transmit Idle Code Definition Register 26 (E1 Mode Only) | R/W |
| 13Ah | TIDR27 | Transmit Idle Code Definition Register 27 (E1 Mode Only) | R/W |
| 13Bh | TIDR28 | Transmit Idle Code Definition Register 28 (E1 Mode Only) | R/W |
| 13Ch | TIDR29 | Transmit Idle Code Definition Register 29 (E1 Mode Only) | R/W |
| 13Dh | TIDR30 | Transmit Idle Code Definition Register 30 (E1 Mode Only) | R/W |
| 13Eh | TIDR31 | Transmit Idle Code Definition Register 31 (E1 Mode Only) | R/W |
| 13Fh | TIDR32 | Transmit Idle Code Definition Register 32 (E1 Mode Only) | R/W |
| 140h | TS1 | Transmit-Signaling Register 1 | R/W |
| 141h | TS2 | Transmit-Signaling Register 2 | R/W |
| 142h | TS3 | Transmit-Signaling Register 3 | R/W |
| 143h | TS4 | Transmit-Signaling Register 4 | R/W |
| 144h | TS5 | Transmit-Signaling Register 5 | R/W |
| 145h | TS6 | Transmit-Signaling Register 6 | R/W |
| 146h | TS7 | Transmit-Signaling Register 7 | R/W |
| 147h | TS8 | Transmit-Signaling Register 8 | R/W |
| 148h | TS9 | Transmit-Signaling Register 9 | R/W |
| 149h | TS10 | Transmit-Signaling Register 10 | R/W |
| 14Ah | TS11 | Transmit-Signaling Register 11 | R/W |
| 14Bh | TS12 | Transmit-Signaling Register 12 | R/W |
| 14Ch | TS13 | Transmit-Signaling Register 13 | R/W |
| 14Dh | TS14 | Transmit-Signaling Register 14 | R/W |
| 14Eh | TS15 | Transmit-Signaling Register 15 | R/W |
| 14Fh | TS16 | Transmit-Signaling Register 16 | R/W |
| 150h | TCICE1 | Transmit Channel Idle Code Enable Register 1 | R/W |
| 151h | TCICE2 | Transmit Channel Idle Code Enable Register 2 | R/W |
| 152h | TCICE3 | Transmit Channel Idle Code Enable Register 3 | R/W |
| 153h | TCICE4 | Transmit Channel Idle Code Enable Register 4 (E1 Mode Only) | R/W |
| 154h–161h | — | Reserved | — |
| 162h | T1TFDL | Transmit FDL Register (T1 Mode Only) | R/W |
| 163h | T1TBOC | Transmit BOC Register (T1 Mode Only) | R/W |
| 164h | T1TSLC1 | Transmit SLC-96 Data Link Register 1 (T1 Mode) | R/W |
| | E1TAF | Transmit Align Frame Register (E1 Mode) | |
| 165h | T1TSLC2 | Transmit SLC-96 Data Link Register 2 (T1 Mode) | R/W |
| | E1TNAF | Transmit Non-Align Frame Register (E1 Mode) | |
| 166h | T1TSLC3 | Transmit SLC-96 Data Link Register 3 (T1 Mode) | R/W |
| | E1TSiAF | Transmit Si Bits of the Align Frame Register (E1 Mode) | |
| 167h | E1TSiNAF | Transmit Si Bits of the Non-Align Frame Register (E1 Mode Only) | R/W |
| 168h | E1TRA | Transmit Remote Alarm Register (E1 Mode) | R/W |

| FRAMER REGISTER LIST | | | |
|----------------------|-------------------------|---|-----|
| ADDRESS | NAME | DESCRIPTION | R/W |
| 169h | E1TSa4 | Transmit Sa4 Bits Register (E1 Mode Only) | R/W |
| 16Ah | E1TSa5 | Transmit Sa5 Bits Register (E1 Mode Only) | R/W |
| 16Bh | E1TSa6 | Transmit Sa6 Bits Register (E1 Mode Only) | R/W |
| 16Ch | E1TSa7 | Transmit Sa7 Bits Register (E1 Mode Only) | R/W |
| 16Dh | E1RSa8 | Receive Sa8 Bits Register (E1 Mode Only) | R/W |
| 16Eh–17Fh | — | Reserved | — |
| 180h | TMMR | Transmit Master Mode Register | R/W |
| 181h | TCR1 | Transmit Control Register 1 (T1 Mode) | R/W |
| | TCR1 | Transmit Control Register 1 (E1 Mode) | |
| 182h | TCR2 | Transmit Control Register 2 (T1 Mode) | R/W |
| | TCR2 | Transmit Control Register 2 (E1 Mode) | |
| 183h | TCR3 | Transmit Control Register 3 | R/W |
| 184h | TIOCR | Transmit I/O Configuration Register | R/W |
| 185h | TESCR | Transmit Elastic Store Control Register | R/W |
| 186h | TCR4 | Transmit Control Register 4 (T1 Mode Only) | R/W |
| 187h | THFC | Transmit HDLC FIFO Control Register | R/W |
| 188h | TIBOC | Transmit Interleave Bus Operation Control Register | R/W |
| 189h | TDS0SEL | Transmit DS0 Channel Monitor Select Register | R/W |
| 18Ah | TXPC | Transmit Expansion Port Control Register | R/W |
| 18Bh | TBPBS | Transmit BERT Port Bit Suppress Register | R/W |
| 18Ch–18Dh | — | Reserved | — |
| 18Eh | TSYNCC | Transmit Synchronizer Control Register | R/W |
| 18F | — | Reserved | — |
| 190h | TLS1 | Transmit Latched Status Register 1 | R/W |
| 191h | TLS2 | Transmit Latched Status Register 2 (HDLC) | R/W |
| 192h | TLS3 | Transmit Latched Status Register 3 (Synchronizer) | R/W |
| 193h–19Eh | — | Reserved | — |
| 19Fh | TIIR | Transmit Interrupt Information Register | R/W |
| 1A0h | TIM1 | Transmit Interrupt Mask Register 1 | R/W |
| 1A1h | TIM2 | Transmit Interrupt Mask Register 2 (HDLC) | R/W |
| 1A2h | TIM3 | Transmit Interrupt Mask Register 3 (Synchronizer) | R/W |
| 1A3h–1ABh | — | Reserved | — |
| 1ACh | T1TCD1 | Transmit Code Definition Register 1 (T1 Mode Only) | R/W |
| 1ADh | T1TCD2 | Transmit Code Definition Register 2 (T1 Mode Only) | R/W |
| 1AEh–1B0h | — | Reserved | — |
| 1B1h | TRTS2 | Transmit Real-Time Status Register 2 (HDLC) | R |
| 1B2h | — | Reserved | — |
| 1B3h | TFBA | Transmit HDLC FIFO Buffer Available | R |
| 1B4h | THF | Transmit HDLC FIFO Register | W |
| 1B5h–1BhA | — | Reserved | — |
| 1BBh | TDS0M | Transmit DS0 Monitor Register | R |
| 1BCh–1BFh | — | Reserved | — |
| 1C0h | TBCS1 | Transmit Blank Channel Select Register 1 | R/W |
| 1C1h | TBCS2 | Transmit Blank Channel Select Register 2 | R/W |
| 1C2h | TBCS3 | Transmit Blank Channel Select Register 3 | R/W |
| 1C3h | TBCS4 | Transmit Blank Channel Select Register 4 (E1 Mode Only) | R/W |
| 1C4h | TCBR1 | Transmit Channel Blocking Register 1 | R/W |
| 1C5h | TCBR2 | Transmit Channel Blocking Register 2 | R/W |
| 1C6h | TCBR3 | Transmit Channel Blocking Register 3 | R/W |
| 1C7h | TCBR4 | Transmit Channel Blocking Register 4 (E1 Mode Only) | R/W |
| 1C8h | THSCS1 | Transmit Hardware-Signaling Channel Select Register 1 | R/W |
| 1C9h | THSCS2 | Transmit Hardware-Signaling Channel Select Register 2 | R/W |

| FRAMER REGISTER LIST | | | |
|----------------------|------------------------|--|-----|
| ADDRESS | NAME | DESCRIPTION | R/W |
| 1CAh | THSCS3 | Transmit Hardware-Signaling Channel Select Register 3 | R/W |
| 1CBh | THSCS4 | Transmit Hardware-Signaling Channel Select Register 4 (E1 Mode Only) | R/W |
| 1CCh | TGCCS1 | Transmit Gapped-Clock Channel Select Register 1 | R/W |
| 1CDh | TGCCS2 | Transmit Gapped-Clock Channel Select Register 2 | R/W |
| 1CEh | TGCCS3 | Transmit Gapped-Clock Channel Select Register 3 | R/W |
| 1CFh | TGCCS4 | Transmit Gapped-Clock Channel Select Register 4 (E1 Mode Only) | R/W |
| 1D0h | PCL1 | Per-Channel Loopback Enable Register 1 | R/W |
| 1D1h | PCL2 | Per-Channel Loopback Enable Register 2 | R/W |
| 1D2h | PCL3 | Per-Channel Loopback Enable Register 3 | R/W |
| 1D3h | PCL4 | Per-Channel Loopback Enable Register 4 (E1 Mode Only) | R/W |
| 1D4h | TBPCS1 | Transmit BERT Port Channel Select Register 1 | R/W |
| 1D5h | TBPCS2 | Transmit BERT Port Channel Select Register 2 | R/W |
| 1D6h | TBPCS3 | Transmit BERT Port Channel Select Register 3 | R/W |
| 1D7h | TBPCS4 | Transmit BERT Port Channel Select Register 4 (E1 Mode Only) | R/W |
| 1D8h–1FFh | — | Reserved | — |

9.1.3 LIU and BERT Register List

Table 9-4. LIU Register List

| LIU REGISTER LIST | | |
|-------------------|------------------------|---|
| ADDRESS | NAME | DESCRIPTION |
| 1000h | LTRCR | LIU Transmit Receive Control Register |
| 1001h | LTITSR | LIU Transmit Impedance and Pulse Shape Selection Register |
| 1002h | LMCR | LIU Maintenance Control Register |
| 1003h | LRSR | LIU Real Status Register |
| 1004h | LSIMR | LIU Status Interrupt Mask Register |
| 1005h | LLSR | LIU Latched Status Register |
| 1006h | LRSL | LIU Receive Signal Level Register |
| 1007 | LRISMR | LIU Receive Impedance and Sensitivity Monitor Register |
| 1008h–101Fh | — | Reserved |

Table 9-5. BERT Register List

| BERT REGISTER LIST | | |
|--------------------|----------------------|---|
| ADDRESS | NAME | DESCRIPTION |
| 1100h | BAWC | BERT Alternating Word Count Rate Register |
| 1101h | BRP1 | BERT Repetitive Pattern Set Register 1 |
| 1102h | BRP2 | BERT Repetitive Pattern Set Register 2 |
| 1103h | BRP3 | BERT Repetitive Pattern Set Register 3 |
| 1104h | BRP4 | BERT Repetitive Pattern Set Register 4 |
| 1105h | BC1 | BERT Control Register 1 |
| 1106h | BC2 | BERT Control Register 2 |
| 1107h | BBC1 | BERT Bit Count Register 1 |
| 1108h | BBC2 | BERT Bit Count Register 2 |
| 1109h | BBC3 | BERT Bit Count Register 3 |
| 110Ah | BBC4 | BERT Bit Count Register 4 |
| 110Bh | BEC1 | BERT Error Count Register 1 |
| 110Ch | BEC2 | BERT Error Count Register 2 |
| 110Dh | BEC3 | BERT Error Count Register 3 |
| 110Eh | BLSR | BERT Latched Status Register |
| 110Fh | BSIM | BERT Status Interrupt Mask Register |

9.2 Register Bit Maps

9.2.1 Global Register Bit Map

Table 9-6. Global Register Bit Map

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|------|-----------------------|-----------|-----------|-----------|-----------|----------|---------|------------|--------|
| 0F0h | GTCR1 | — | — | RLOFLTS | GIBO | — | BWE | GCLE | GIPI |
| 0F1h | GFCCR | IBOMS1 | IBOMS0 | BPCLK1 | BPCLK0 | RFLOSSFS | RFMSS | TCBCS | RCBCS |
| 0F2h | GTCR2 | — | — | — | — | — | LOSS | TSSYNCISEL | — |
| 0F3h | GTCCR | BPREFSEL3 | BPREFSEL2 | BPREFSEL1 | BPREFSEL0 | BFREQSEL | FREQSEL | MPS1 | MPS0 |
| 0F4h | — | — | — | — | — | — | — | — | — |
| 0F5h | GLSRR | — | — | — | — | LSRST4 | LSRST3 | LSRST2 | LSRST1 |
| 0F6h | GFSRR | — | — | — | — | FSRST4 | FSRST3 | FSRST2 | FSRST1 |
| 0F7h | — | — | — | — | — | — | — | — | — |
| 0F8h | IDR | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
| 0F9h | GFISR | — | — | — | — | FIS4 | FIS3 | FIS2 | FIS1 |
| 0Fah | GBISR | — | — | — | — | BIS4 | BIS3 | BIS2 | BIS1 |
| 0FBh | GLISR | — | — | — | — | LIS4 | LIS3 | LIS2 | LIS1 |
| 0FCh | GFIMR | — | — | — | — | FIM4 | FIM3 | FIM2 | FIM1 |
| 0FDh | GBIMR | — | — | — | — | BIM4 | BIM3 | BIM2 | BIM1 |
| 0FEh | GLIMR | — | — | — | — | LIM4 | LIM3 | LIM2 | LIM1 |

9.2.2 Framer Register Bit Map

[Table 9-7](#) contains the framer registers of the DS26524. Some registers have dual functionality based on the selection of T1/J1 or E1 operating mode in the [RMMR](#) and [TMMR](#) registers. These dual-function registers are shown below using two lines of text. The first line of text is the bit functionality for T1/J1 mode. The second line is the bit functionality in E1 mode, in *italics*. Bits that are not used for an operating mode are noted with a dash “—”. When there is only one set of bit definitions listed for a register, the bit functionality does not change with respect to the selection of T1/J1 or E1 mode. All registers not listed are reserved and should be initialized with a value of 00h for proper operation. The addresses shown are for Framer 1. Addresses for Framer 2 to 4 can be calculated using the following formula: Address for Framer N = (Framer 1 address + (N - 1) x 200h).

Table 9-7. Framer Register Bit Map

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|------|--------------------------|-----------|-----------|-----------|---------------|---------------|---------------|---------------|---------------|
| 010h | RHC | RCRCD | RHR | RHMS | RHCS4 | RHCS3 | RHCS2 | RHCS1 | RHCS0 |
| 011h | RHBSE | BSE8 | BSE7 | BSE6 | BSE5 | BSE4 | BSE3 | BSE2 | BSE1 |
| 012h | RDS0SEL | — | — | — | RCM4 | RCM3 | RCM2 | RCM1 | RCM0 |
| 013h | RSIGC | — | — | — | RFSA1 | — | RSFF | RSFE | RSIE |
| | | — | — | — | CASMS | — | RSFF | RSFE | RSEI |
| 014h | T1RCR2 | — | — | — | RSLC96 | OOF2 | OOF1 | RAIIE | RD4RM |
| | E1RSAIMR | — | — | — | <i>RSa4IM</i> | <i>RSa5IM</i> | <i>RSa6IM</i> | <i>RSa7IM</i> | <i>RSa8IM</i> |
| 015h | T1RBOCC | RBR | — | RBD1 | RBD0 | — | RBF1 | RBF0 | — |
| 020h | RIDR1 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 021h | RIDR2 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 022h | RIDR3 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 023h | RIDR4 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 024h | RIDR5 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 025h | RIDR6 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 026h | RIDR7 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 027h | RIDR8 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 028h | RIDR9 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 029h | RIDR10 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 02Ah | RIDR11 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 02Bh | RIDR12 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 02Ch | RIDR13 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 02Dh | RIDR14 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 02Eh | RIDR15 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 02Fh | RIDR16 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 030h | RIDR17 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 031h | RIDR18 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 032h | RIDR19 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 033h | RIDR20 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 034h | RIDR21 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 035h | RIDR22 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 036h | RIDR23 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 037h | RIDR24 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 038h | T1RSAOI1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| | <i>RIDR25</i> | <i>C7</i> | <i>C6</i> | <i>C5</i> | <i>C4</i> | <i>C3</i> | <i>C2</i> | <i>C1</i> | <i>C0</i> |
| 039h | T1RSAOI2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| | <i>RIDR26</i> | <i>C7</i> | <i>C6</i> | <i>C5</i> | <i>C4</i> | <i>C3</i> | <i>C2</i> | <i>C1</i> | <i>C0</i> |
| 03Ah | T1RSAOI3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| | <i>RIDR27</i> | <i>C7</i> | <i>C6</i> | <i>C5</i> | <i>C4</i> | <i>C3</i> | <i>C2</i> | <i>C1</i> | <i>C0</i> |

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|------|--------------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| 03Bh | RIDR28 | — | — | — | — | — | — | — | — |
| | | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 03Ch | T1RDMWE1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| | RIDR29 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 03Dh | T1RDMWE2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| | RIDR30 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 03Eh | T1RDMWE3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| | RIDR31 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 03Fh | RIDR32 | — | — | — | — | — | — | — | — |
| | | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 040h | RS1 | CH1-A | CH1-B | CH1-C | CH1-D | CH13-A | CH13-B | CH13-C | CH13-D |
| | | 0 | 0 | 0 | 0 | X | Y | X | X |
| 041h | RS2 | CH2-A | CH2-B | CH2-C | CH2-D | CH14-A | CH14-B | CH14-C | CH14-D |
| | | CH1-A | CH1-B | CH1-C | CH1-D | CH16-A | CH16-B | CH16-C | CH16-D |
| 042h | RS3 | CH3-A | CH3-B | CH3-C | CH3-D | CH15-A | CH15-B | CH15-C | CH15-D |
| | | CH2-A | CH2-B | CH2-C | CH2-D | CH17-A | CH17-B | CH17-C | CH17-D |
| 043h | RS4 | CH4-A | CH4-B | CH4-C | CH4-D | CH16-A | CH16-B | CH16-C | CH16-D |
| | | CH3-A | CH3-B | CH3-C | CH3-D | CH18-A | CH18-B | CH18-C | CH18-D |
| 044h | RS5 | CH5-A | CH5-B | CH5-C | CH5-D | CH17-A | CH17-B | CH17-C | CH17-D |
| | | CH4-A | CH4-B | CH4-C | CH4-D | CH19-A | CH19-B | CH19-C | CH19-D |
| 045h | RS6 | CH6-A | CH6-B | CH6-C | CH6-D | CH18-A | CH18-B | CH18-C | CH18-D |
| | | CH5-A | CH5-B | CH5-C | CH5-D | CH20-A | CH20-B | CH20-C | CH20-D |
| 046h | RS7 | CH7-A | CH7-B | CH7-C | CH7-D | CH19-A | CH19-B | CH19-C | CH19-D |
| | | CH6-A | CH6-B | CH6-C | CH6-D | CH21-A | CH21-B | CH21-C | CH21-D |
| 047h | RS8 | CH8-A | CH8-B | CH8-C | CH8-D | CH20-A | CH20-B | CH20-C | CH20-D |
| | | CH7-A | CH7-B | CH7-C | CH7-D | CH22-A | CH22-B | CH22-C | CH22-D |
| 048h | RS9 | CH9-A | CH9-B | CH9-C | CH9-D | CH21-A | CH21-B | CH21-C | CH21-D |
| | | CH8-A | CH8-B | CH8-C | CH8-D | CH23-A | CH23-B | CH23-C | CH23-D |
| 049h | RS10 | CH10-A | CH10-B | CH10-C | CH10-D | CH22-A | CH22-B | CH22-C | CH22-D |
| | | CH9-A | CH9-B | CH9-C | CH9-D | CH24-A | CH24-B | CH24-C | CH24-D |
| 04Ah | RS11 | CH11-A | CH11-B | CH11-C | CH11-D | CH23-A | CH23-B | CH23-C | CH23-D |
| | | CH10-A | CH10-B | CH10-C | CH10-D | CH25-A | CH25-B | CH25-C | CH25-D |
| 04Bh | RS12 | CH12-A | CH12-B | CH12-C | CH12-D | CH24-A | CH24-B | CH24-C | CH24-D |
| | | CH11-A | CH11-B | CH11-C | CH11-D | CH26-A | CH26-B | CH26-C | CH26-D |
| 04Ch | RS13 | — | — | — | — | — | — | — | — |
| | | CH12-A | CH12-B | CH12-C | CH12-D | CH27-A | CH27-B | CH27-C | CH27-D |
| 04Dh | RS14 | — | — | — | — | — | — | — | — |
| | | CH13-A | CH13-B | CH13-C | CH13-D | CH28-A | CH28-B | CH28-C | CH28-D |
| 04Eh | RS15 | — | — | — | — | — | — | — | — |
| | | CH14-A | CH14-B | CH14-C | CH14-D | CH29-A | CH29-B | CH29-C | CH29-D |
| 04Fh | RS16 | — | — | — | — | — | — | — | — |
| | | CH15-A | CH15-B | CH15-C | CH15-D | CH30-A | CH30-B | CH30-C | CH30-D |
| 050h | LCVCR1 | LCVC15 | LCVC14 | LCVC13 | LCVC12 | LCVC11 | LCVC10 | LCVC9 | LCCV8 |
| 051h | LCVCR2 | LCVC7 | LCVC6 | LCVC5 | LCVC4 | LCVC3 | LCVC2 | LCVC1 | LCVC0 |
| 052h | PCVCR1 | PCVC15 | PCVC14 | PCVC13 | PCVC12 | PCVC11 | PCVC10 | PCVC9 | PCVC8 |
| 053h | PCVCR2 | PCVC7 | PCVC6 | PCVC5 | PCVC4 | PCVC3 | PCVC2 | PCVC1 | PCVC0 |
| 054h | FOSCR1 | FOS15 | FOS14 | FOS13 | FOS12 | FOS11 | FOS10 | FOS9 | FOS8 |
| 055h | FOSCR2 | FOS7 | FOS6 | FOS5 | FOS4 | FOS3 | FOS2 | FOS1 | FOS0 |

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|------|---------------------------|---------|-----------|---------|---------|---------|--------|---------|--------|
| 056h | E1EBCR1 | EB15 | EB14 | EB13 | EB12 | EB11 | EB10 | EB9 | EB8 |
| 057h | E1EBCR2 | EB7 | EB6 | EB5 | EB4 | EB3 | EB2 | EB1 | EB0 |
| 060h | RDS0M | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 |
| 061h | — | — | — | — | — | — | — | — | — |
| 062h | T1RFDL | RFDL7 | RFDL6 | RFDL5 | RFDL4 | RFDL3 | RFDL2 | RFDL1 | RFDL0 |
| | E1RRTS7 | CSC5 | CSC4 | CSC3 | CSC2 | CSC0 | CRC4SA | CASSA | FASSA |
| 063h | T1RBOC | — | — | RBOC5 | RBOC4 | RBOC3 | RBOC2 | RBOC1 | RBOC0 |
| 064h | T1RSLC1 | C8 | C7 | C6 | C5 | C4 | C3 | C2 | C1 |
| | E1RAF | Si | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 065h | T1RSLC2 | M2 | M1 | S=0 | S=1 | S=0 | C11 | C10 | C9 |
| | E1RNAF | Si | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| 066h | T1RSLC3 | S=1 | S4 | S3 | S2 | S1 | A2 | A1 | M3 |
| | E1RSiAF | SiF14 | SiF12 | SiF10 | SiF8 | SiF6 | SiF4 | SiF2 | SiF0 |
| 067h | E1RSiNAF | SiF15 | SiF13 | SiF11 | SiF9 | SiF7 | SiF5 | SiF3 | SiF1 |
| 068h | E1RRA | RRAF15 | RRAF13 | RRAF11 | RRAF9 | RRAF7 | RRAF5 | RRAF3 | RRAF1 |
| 069h | E1RSa4 | RSa4F15 | RSa4F13 | RSa4F11 | RSa4F9 | RSa4F7 | RSa4F5 | RSa4F3 | RSa4F1 |
| 06Ah | E1RSa5 | RSa5F15 | RSa5F13 | RSa5F11 | RSa5F9 | RSa5F7 | RSa5F5 | RSa5F3 | RSa5F1 |
| 06Bh | E1RSa6 | RSa6F15 | RSa6F13 | RSa6F11 | RSa6F9 | RSa6F7 | RSa6F5 | RSa6F3 | RSa6F1 |
| 06Ch | E1RSa7 | RSa7F15 | RSa7F13 | RSa7F11 | RSa7F9 | RSa7F7 | RSa7F5 | RSa7F3 | RSa7F1 |
| 06Dh | E1RSa8 | RSa8F15 | RSa8F13 | RSa8F11 | RSa8F9 | RSa8F7 | RSa8F5 | RSa8F3 | RSa8F1 |
| 06Eh | SaBITS | — | — | — | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| 06Fh | Sa6CODE | — | — | — | — | Sa6n | Sa6n | Sa6n | Sa6n |
| 080h | RMMR | FRM_EN | INIT_DONE | — | — | — | — | SFTRST | T1/E1 |
| 081h | RCR1 (T1) | SYNCT | RB8ZS | RFM | ARC | SYNCC | RJC | SYNCE | RESYNC |
| | RCR1 (E1) | — | RHDB3 | RSIGM | RG802 | RCRC4 | FRC | SYNCE | RESYNC |
| 082h | T1RIBCC | — | — | RUP2 | RUP1 | RUP0 | RDN2 | RDN1 | RDN0 |
| | E1RCR2 | RSa8S | RSa7S | RSa6S | RSa5S | RSa4S | — | — | RLOSA |
| 083h | RCR3 | IDF | — | RSERC | — | — | — | PLB | FLB |
| 084h | RIOCR | RCLKINV | RSYNCLINV | H100EN | RSCLKM | RSMS | RSIO | RSMS2 | RSMS1 |
| | | RCLKINV | RSYNCLINV | H100EN | RSCLKM | — | RSIO | RSMS2 | RSMS1 |
| 085h | RESCR | RDATFMT | RGCLKEN | — | RSZS | RESALGN | RESR | RESMDM | RESE |
| 086h | ERCNT | 1SECS | MCUS | MECU | ECUS | EAMS | FSBE | MOSCRF | LCVCRF |
| | | 1SECS | MCUS | MECU | ECUS | EAMS | — | — | LCVCRF |
| 087h | RHFC | — | — | — | — | — | — | RFHWM1 | RFHWM0 |
| 088h | RIBOC | — | IBS1 | IBS0 | IBOSEL | IBOEN | DA2 | DA1 | DA0 |
| 089h | T1RSCC | — | — | — | — | — | RSC2 | RSC1 | RSC0 |
| 08Ah | RXPC | — | — | — | — | — | RBPDIR | RBPDIR | RBPEN |
| | | — | — | — | — | — | RBPDIR | — | RBPEN |
| 08Bh | RBPBS | BPBSE8 | BPBSE7 | BPBSE6 | BPBSE5 | BPBSE4 | BPBSE3 | BPBSE2 | BPBSE1 |
| 090h | RLS1 | RRAIC | RAISC | RLOSC | RLOFC | RRAID | RAISD | RLOSD | RLOFD |
| 091h | RLS2 (T1) | RPDV | — | COFA | 8ZD | 16ZD | SEFE | B8ZS | FBE |
| | RLS2 (E1) | — | CRCRC | CASRC | FASRC | RSA1 | RSA0 | RCMF | RAF |
| 092h | RLS3 (T1) | LORCC | LSPC | LDNC | LUPC | LORCD | LSPD | LDND | LUPD |
| | RLS3 (E1) | LORCC | — | V52LNKC | RDMAC | LORCD | — | V52LNKD | RDMAD |
| 093h | RLS4 | RESF | RESEM | RSLIP | — | RSCOS | 1SEC | TIMER | RMF |
| 094h | RLS5 | — | — | ROVR | RHOBT | RPE | RPS | RHWMS | RNES |
| 096h | RLS7 (T1) | — | — | RRAI-CI | RAIS-CI | RSLC96 | RFDLF | BC | BD |
| | RLS7 (E1) | — | — | — | — | — | — | Sa6CD | SaXCD |

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|------|----------------------------|--------------|-------------|----------------|--------------|--------------|-------------|----------------|--------------------|
| 097h | — | — | — | — | — | — | — | — | — |
| 098h | RSS1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 099h | RSS2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 09Ah | RSS3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 09Bh | RSS4 | — | — | — | — | — | — | — | — |
| | | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> |
| 09Ch | T1RSCD1 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| | | — | — | — | — | — | — | — | — |
| 09Dh | T1RSCD2 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| | | — | — | — | — | — | — | — | — |
| 09Fh | RIIR | — | RLS7 | RLS6* | RLS5 | RLS4 | RLS3 | RLS2** | RLS1 |
| 0A0h | RIM1 | RRAIC | RAISC | RLOSC | RLOFC | RRAID | RAISD | RLOSD | RLOFD |
| 0A1h | RIM2 | — | — | — | — | — | — | — | — |
| | | — | — | — | — | <i>RSA1</i> | <i>RSA0</i> | <i>RCMF</i> | <i>RAF</i> |
| 0A2h | RIM3 (T1) | LORCC | LSPC | LDNC | LUPC | LORCD | LSPD | LDND | LUPD |
| | RIM3 (E1) | <i>LORCC</i> | — | <i>V52LNKC</i> | <i>RDMAC</i> | <i>LORCD</i> | — | <i>V52LNKD</i> | <i>RDMAD</i> |
| 0A3h | RIM4 | RESF | RESEM | RSLIP | — | RSCOS | 1SEC | TIMER | RMF |
| 0A4h | RIM5 | — | — | ROVR | RHOBT | RPE | RPS | RHWMS | RNES |
| 0A6h | RIM7 (T1) | — | — | RRAI-CI | RAIS-CI | RSLC96 | RFDLF | BC | BD |
| | RIM7 (E1) | — | — | — | — | — | — | <i>Sa6CD</i> | <i>SaXCD</i> |
| 0A8h | RSCSE1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 0A9h | RSCSE2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 0AAh | RSCSE3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 0Abh | RSCSE4 | — | — | — | — | — | — | — | — |
| | | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> |
| 0ACh | T1RUPCD1 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| | | — | — | — | — | — | — | — | — |
| 0ADh | T1RUPCD2 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| | | — | — | — | — | — | — | — | — |
| 0AEh | T1RDNCD1 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| | | — | — | — | — | — | — | — | — |
| 0AFh | T1RDNCD2 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| | | — | — | — | — | — | — | — | — |
| 0B0h | RRTS1 | — | — | — | — | RRAI | RAIS | RLOS | RLOF |
| 0B2h | RRTS3 (T1) | — | — | — | — | LORC | LSP | LDN | LUP |
| | RRTS3 (E1) | — | — | — | — | <i>LORC</i> | — | <i>V52LNK</i> | <i>RDMA</i> |
| 0B4h | RRTS5 | — | PS2 | PS1 | PS0 | — | — | RHWM | RNE |
| 0B5h | RHPBA | MS | RPBA6 | RPBA5 | RPBA4 | RPBA3 | RPBA2 | RPBA1 | RPBA0 |
| 0B6h | RHF | RHD7 | RHD6 | RHD5 | RHD4 | RHD3 | RHD2 | RHD1 | RHD0 |
| 0C0h | RBCS1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 0C1h | RBCS2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 0C2h | RBCS3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 0C3h | RBCS4 | — | — | — | — | — | — | — | — |
| | | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> |
| 0C4h | RCBR1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 0C5h | RCBR2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 0C6h | RCBR3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 0C7h | RCBR4 | — | — | — | — | — | — | — | — |
| | | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25(F-bit)</i> |
| 0C8h | RS11 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|------|------------------------|-------------|-------------|--------------|--------------|--------------|--------------|--------------|--------------------|
| 0C9h | RSI2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 0CAh | RSI3 | CH24 | CH23 | CH22 | CH21 | CH200 | CH19 | CH18 | CH17 |
| 0CBh | RSI4 | — | — | — | — | — | — | — | — |
| | | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> |
| 0CCh | RGCCS1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 0CDh | RGCCS2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 0CEh | RGCCS3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 0CFh | RGCCS4 | — | — | — | — | — | — | — | — |
| | | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25(F-bit)</i> |
| 0D0h | RCICE1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 0D1h | RCICE2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 0D2h | RCICE3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 0D3h | RCICE4 | — | — | — | — | — | — | — | — |
| | | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> |
| 0D4h | RBPCS1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 0D5h | RBPCS2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 0D6h | RBPCS3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 0D7h | RBPCS4 | — | — | — | — | — | — | — | — |
| | | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> |
| 110h | THC1 | NOFS | TEOML | THR | THMS | TFS | TEOM | TZSD | TCRCD |
| 111h | THBSE | TBSE8 | TBSE7 | TBSE6 | TBSE5 | TBSE4 | TBSE3 | TBSE2 | TBSE1 |
| 113h | THC2 | TABT | SBOC | THCEN | THCS4 | THCS3 | THCS2 | THCS1 | THCS0 |
| | | <i>TABT</i> | — | <i>THCEN</i> | <i>THCS4</i> | <i>THCS3</i> | <i>THCS2</i> | <i>THCS1</i> | <i>THCS0</i> |
| 118h | SSIE1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 119h | SSIE2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 11Ah | SSIE3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 11Bh | SSIE4 | — | — | — | — | — | — | — | — |
| | | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> |
| 120h | TIDR1 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 121h | TIDR2 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 122h | TIDR3 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 123h | TIDR4 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 124h | TIDR5 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 125h | TIDR6 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 126h | TIDR7 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 127h | TIDR8 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 128h | TIDR9 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 129h | TIDR10 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 12Ah | TIDR11 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 12Bh | TIDR12 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 12Ch | TIDR13 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 12Dh | TIDR14 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 12Eh | TIDR15 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 12Fh | TIDR16 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 130h | TIDR17 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 131h | TIDR18 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 132h | TIDR19 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 133h | TIDR20 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 134h | TIDR21 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 135h | TIDR22 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 136h | TIDR23 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 137h | TIDR24 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 138h | TIDR25 | — | — | — | — | — | — | — | — |
| | | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 139h | TIDR26 | — | — | — | — | — | — | — | — |
| | | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 13Ah | TIDR27 | — | — | — | — | — | — | — | — |
| | | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 13Bh | TIDR28 | — | — | — | — | — | — | — | — |
| | | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 13Ch | TIDR29 | — | — | — | — | — | — | — | — |
| | | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 13Dh | TIDR30 | — | — | — | — | — | — | — | — |
| | | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 13Eh | TIDR31 | — | — | — | — | — | — | — | — |
| | | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 13Fh | TIDR32 | — | — | — | — | — | — | — | — |
| | | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 140h | TS1 | CH1-A | CH1-B | CH1-C | CH1-D | CH13-A | CH13-B | CH13-C | CH13-D |
| | | 0 | 0 | 0 | 0 | X | Y | X | X |
| 141h | TS2 | CH2-A | CH2-B | CH2-C | CH2-D | CH14-A | CH14-B | CH14-C | CH14-D |
| | | CH1-A | CH1-B | CH1-C | CH1-D | CH16-A | CH16-B | CH16-C | CH16-D |
| 142h | TS3 | CH3-A | CH3-B | CH3-C | CH3-D | CH15-A | CH15-B | CH15-C | CH15-D |
| | | CH2-A | CH2-B | CH2-C | CH2-D | CH17-A | CH17-B | CH17-C | CH17-D |
| 143h | TS4 | CH4-A | CH4-B | CH4-C | CH4-D | CH16-A | CH16-B | CH16-C | CH16-D |
| | | CH3-A | CH3-B | CH3-C | CH3-D | CH18-A | CH18-B | CH18-C | CH18-D |
| 144h | TS5 | CH5-A | CH5-B | CH5-C | CH5-D | CH17-A | CH17-B | CH17-C | CH17-D |
| | | CH4-A | CH4-B | CH4-C | CH4-D | CH19-A | CH19-B | CH19-C | CH19-D |
| 145h | TS6 | CH6-A | CH6-B | CH6-C | CH6-D | CH18-A | CH18-B | CH18-C | CH18-D |
| | | CH5-A | CH5-B | CH5-C | CH5-D | CH20-A | CH20-B | CH20-C | CH20-D |
| 146h | TS7 | CH7-A | CH7-B | CH7-C | CH7-D | CH19-A | CH19-B | CH19-C | CH19-D |
| | | CH6-A | CH6-B | CH6-C | CH6-D | CH21-A | CH21-B | CH21-C | CH21-D |
| 147h | TS8 | CH8-A | CH8-B | CH8-C | CH8-D | CH20-A | CH20-B | CH20-C | CH20-D |
| | | CH7-A | CH7-B | CH7-C | CH7-D | CH22-A | CH22-B | CH22-C | CH22-D |
| 148h | TS9 | CH9-A | CH9-B | CH9-C | CH9-D | CH21-A | CH21-B | CH21-C | CH21-D |
| | | CH8-A | CH8-B | CH8-C | CH8-D | CH23-A | CH23-B | CH23-C | CH23-D |
| 149h | TS10 | CH10-A | CH10-B | CH10-C | CH10-D | CH22-A | CH22-B | CH22-C | CH22-D |
| | | CH9-A | CH9-B | CH9-C | CH9-D | CH24-A | CH24-B | CH24-C | CH24-D |
| 14Ah | TS11 | CH11-A | CH11-B | CH11-C | CH11-D | CH23-A | CH23-B | CH23-C | CH23-D |
| | | CH10-A | CH10-B | CH10-C | CH10-D | CH25-A | CH25-B | CH25-C | CH25-D |
| 14Bh | TS12 | CH12-A | CH12-B | CH12-C | CH12-D | CH24-A | CH24-B | CH24-C | CH24-D |
| | | CH11-A | CH11-B | CH11-C | CH11-D | CH26-A | CH26-B | CH26-C | CH26-D |
| 14Ch | TS13 | — | — | — | — | — | — | — | — |
| | | CH12-A | CH12-B | CH12-C | CH12-D | CH27-A | CH27-B | CH27-C | CH27-D |
| 14Dh | TS14 | — | — | — | — | — | — | — | — |
| | | CH13-A | CH13-B | CH13-C | CH13-D | CH28-A | CH28-B | CH28-C | CH28-D |

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|------|--|---------|-----------|-----------|--------|---------|--------|--------|--------|
| 14Eh | TS15 | — | — | — | — | — | — | — | — |
| | | CH14-A | CH14-B | CH14-C | CH14-D | CH29-A | CH29-B | CH29-C | CH29-D |
| 14Fh | TS16 | — | — | — | — | — | — | — | — |
| | | CH15-A | CH15-B | CH15-C | CH15-D | CH30-A | CH30-B | CH30-C | CH30-D |
| 150h | TCICE1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 151h | TCICE2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 152h | TCICE3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 153h | TCICE4 | — | — | — | — | — | — | — | — |
| | | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| 162h | T1TFDL | TFDL7 | TFDL6 | TFDL5 | TFDL4 | TFDL3 | TFDL2 | TFDL1 | TFDL0 |
| | | — | — | — | — | — | — | — | — |
| 163h | T1TBOC | — | — | TBOC5 | TBOC4 | TBOC3 | TBOC2 | TBOC1 | TBOC0 |
| | | — | — | — | — | — | — | — | — |
| 164h | T1TSLC1 E1TAF | C8 | C7 | C6 | C5 | C4 | C3 | C2 | C1 |
| | | Si | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 165h | T1TSLC2 E1TNAF | M2 | M1 | S=0 | S=1 | S=0 | C11 | C10 | C9 |
| | | Si | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| 166h | T1TSLC3 E1TSiAF | S=1 | S4 | S3 | S2 | S1 | A2 | A1 | M3 |
| | | TSiF14 | TSiF12 | TSiF10 | TSiF8 | TSiF6 | TSiF4 | TSiF2 | TSiF0 |
| 167h | E1TSiNAF | — | — | — | — | — | — | — | — |
| | | TsiF15 | TSiF13 | TSiF11 | TSiF9 | TSiF7 | TSiF5 | TSiF3 | TSiF1 |
| 168h | E1TRA | — | — | — | — | — | — | — | — |
| | | TRAF15 | TRAF13 | TRAF11 | TRAF9 | TRAF7 | TRAF5 | TRAF3 | TRAF1 |
| 169h | E1TSa4 | — | — | — | — | — | — | — | — |
| | | TSa4F15 | TSa4F13 | TSa4F11 | TSa4F9 | TSa4F7 | TSa4F5 | TSa4F3 | TSa4F1 |
| 16Ah | E1TSa5 | — | — | — | — | — | — | — | — |
| | | TSa5F15 | TSa5F13 | TSa5F11 | TSa5F9 | TSa5F7 | TSa5F5 | TSa5F3 | TSa5F1 |
| 16Bh | E1TSa6 | — | — | — | — | — | — | — | — |
| | | TSa6F15 | TSa6F13 | TSa6F11 | TSa6F9 | TSa6F7 | TSa6F5 | TSa6F3 | TSa6F1 |
| 16Ch | E1TSa7 | — | — | — | — | — | — | — | — |
| | | TSa7F15 | TSa7F13 | TSa7F11 | TSa7F9 | TSa7F7 | TSa7F5 | TSa7F3 | TSa7F1 |
| 16Dh | E1TSa8 | — | — | — | — | — | — | — | — |
| | | TSa8F15 | TSa8F13 | TSa8F11 | TSa8F9 | TSa8F7 | TSa8F5 | TSa8F3 | TSa8F1 |
| 180h | IMMR | FRM_EN | INIT_DONE | — | — | — | — | SFTRST | T1/E1 |
| 181h | TCR1 (T1) TCR1 (E1) | TJC | TFPT | TCPT | TSSE | GB7S | TB8ZS | TAIS | TRAI |
| | | TTPPT | T16S | TG802 | TSiS | TSA1 | THDB3 | TAIS | TCRC4 |
| 182h | TCR2 (T1) TCR2 (E1) | TFDLS | TSLC96 | — | FBCT2 | FBCT1 | TD4RM | PDE | TB7ZS |
| | | AEBE | AAIS | ARA | Sa4S | Sa5S | Sa6S | Sa7S | Sa8S |
| 183h | TCR3 | ODF | ODM | TCSS1 | TCSS0 | MFRS | TFM | IBPV | TLOOP |
| | | ODF | ODM | TCSS1 | TCSS0 | MFRS | — | IBPV | CRC4R |
| 184h | TIOCR | TCLKINV | TSYNCINV | TSSYNCINV | TSCLKM | TSSM | TSIO | TSDW | TSM |
| | | TCLKINV | TSYNCINV | TSSYNCINV | TSCLKM | TSSM | TSIO | — | TSM |
| 185h | TESCR | TDATFMT | TGCLKEN | — | TSZS | TESALGN | TESR | TESMDM | TESE |
| 186h | TCR4 | — | — | — | — | TRAIM | TAISM | TC1 | TC0 |
| | | — | — | — | — | — | — | — | — |
| 187h | THFC | — | — | — | — | — | — | TFLWM1 | TFLWM2 |
| 188h | TIBOC | — | IBS1 | IBS0 | IBOSEL | IBOEN | DA2 | DA1 | DA0 |
| 189h | TDS0SEL | — | — | — | TCM4 | TCM3 | TCM2 | TCM1 | TCM0 |

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|------|------------------------|--------|--------|--------|--------|--------|--------|--------|-------------|
| 18Ah | TXPC | — | — | — | — | — | TBPDIR | TBPFUS | TBPEN |
| 18Bh | TBPBS | BPBSE8 | BPBSE7 | BPBSE6 | BPBSE5 | BPBSE4 | BPBSE3 | BPBSE2 | BPBSE1 |
| 18Eh | TSYNCC | — | — | — | — | — | TSEN | SYNCE | RESYNC |
| | | — | — | — | — | CRC4 | TSEN | SYNCE | RESYNC |
| 190h | TLS1 | TESF | TESEM | TSLIP | TSLC96 | TPDV | TMF | LOTCC | LOTC |
| | | TESF | TESEM | TSLIP | — | TAF | TMF | LOTCC | LOTC |
| 191h | TLS2 | — | — | — | TFDLE | TUDR | TMEND | TLWMS | TNFS |
| | | — | — | — | — | TUDR | TMEND | TLWMS | TNFS |
| 192h | TLS3 | — | — | — | — | — | — | LOF | LOFD |
| 19Fh | TIIR | — | — | — | — | — | TLS3 | TLS2 | TLS1 |
| 1A0h | TIM1 | TESF | TESEM | TSLIP | TSLC96 | TPDV | TMF | LOTCC | LOTC |
| | | TESF | TESEM | TSLIP | — | TAF | TMF | LOTCC | LOTC |
| 1A1h | TIM2 | — | — | — | TFDLE | TUDR | TMEND | TLWMS | TNFS |
| | | — | — | — | — | TUDR | TMEND | TLWMS | TNFS |
| 1A2h | TIM3 | — | — | — | — | — | — | — | LOFD |
| 1ACh | T1TCD1 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| | | — | — | — | — | — | — | — | — |
| ADh | T1TCD2 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| | | — | — | — | — | — | — | — | — |
| 1B1h | TRTS2 | — | — | — | — | EMPTY | TFULL | TLWMS | TNF |
| 1B3h | TFBA | — | TFBA6 | TFBA5 | TFBA4 | TFBA3 | TFBA2 | TFBA1 | TFBA0 |
| 1B4h | THE | THD7 | THD6 | THD5 | THD4 | THD3 | THD2 | THD1 | THD0 |
| 1BBh | TDSOM | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 |
| 1C0h | TBCS1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 1C1h | TBCS2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 1C2h | TBCS3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 1C3h | TBCS4 | — | — | — | — | — | — | — | — |
| | | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| 1C4h | TCBR1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 1C5h | TCBR2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 1C6h | TCBR3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 1C7h | TCBR4 | — | — | — | — | — | — | — | — |
| | | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25:Fbit |
| 1C8h | THSCS1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 1C9h | THSCS2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 1CAh | THSCS3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 1CBh | THSCS4 | — | — | — | — | — | — | — | — |
| | | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| 1CCh | TGCCS1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 1CDh | TGCCS2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 1CEh | TGCCS3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 1CFh | TGCCS4 | — | — | — | — | — | — | — | — |
| | | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25(F-bit) |
| 1D0h | PCL1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 1D1h | PCL2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 1D2h | PCL3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 1D3h | PCL4 | — | — | — | — | — | — | — | — |
| | | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|------|------------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 1D4h | TBPCS1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 1D5h | TBPCS2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 1D6h | TBPCS3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 1D7h | TBPCS4 | — | — | — | — | — | — | — | — |
| | | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |

*RLS6 is reserved for future use.

**Currently, RLS2 does not create an interrupt, therefore this bit is not used in T1 mode.

9.2.3 LIU Register Bit Map

Table 9-8. LIU Register Bit Map

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|-------|------------------------|---------|----------|--------|--------|---------|--------|---------|--------|
| 1000h | LTRCR | — | — | — | JADS | JAPS1 | JAPS0 | T1J1E1S | LSC |
| 1001h | LTISR | — | TIMPTOFF | TIMPL1 | TIMPL0 | — | L2 | L1 | L0 |
| 1002h | LMCR | TAIS | ATAIS | LLB | ALB | RLB | TPDE | RPDE | TE |
| 1003h | LRSR | — | — | OEQ | UEQ | — | SCS | OCS | LOSS |
| 1004h | LSIMR | JALTCIM | OCCIM | SCCIM | LOSCIM | JALTSIM | OCDIM | SCDIM | LOSDIM |
| 1005h | LLSR | JALTC | OCC | SCC | LOSC | JALTS | OCD | SCD | LOSD |
| 1006h | LRSL | RSL3 | RSL2 | RLS1 | RLS0 | — | — | — | — |
| 1007h | LRISMR | RG703 | RIMPOFF | RIMPM1 | RIMPM0 | RTR | RMONEN | RSMS1 | RSMS0 |

9.2.4 BERT Register Bit Map

Table 9-9. BERT Register Bit Map

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|-------|----------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| 1100h | BAWC | ACNT7 | ACNT6 | ACNT5 | ACNT4 | ACNT3 | ACNT2 | ACNT1 | ACNT0 |
| 1101h | BRP1 | RPAT7 | RPAT6 | RPAT5 | RPAT4 | RPAT3 | RPAT2 | RPAT1 | RPAT0 |
| 1102h | BRP2 | RPAT15 | RPAT14 | RPAT13 | RPAT12 | RPAT11 | RPAT10 | RPAT9 | RPAT8 |
| 1103h | BRP3 | RPAT23 | RPAT22 | RPAT21 | RPAT20 | RPAT19 | RPAT18 | RPAT17 | RPAT16 |
| 1104h | BRP4 | RPAT31 | RPAT30 | RPAT29 | RPAT28 | RPAT27 | RPAT26 | RPAT25 | RPAT24 |
| 1105h | BC1 | TC | TINV | RINV | PS2 | PS1 | PS0 | LC | RESYNC |
| 1106h | BC2 | EIB2 | EIB1 | EIB0 | SBE | RPL3 | RPL2 | RPL1 | RPL0 |
| 1107h | BBC1 | BBC7 | BBC6 | BBC5 | BBC4 | BBC3 | BBC2 | BBC1 | BBC0 |
| 1108h | BBC2 | BBC15 | BBC14 | BBC13 | BBC12 | BBC11 | BBC10 | BBC9 | BBC8 |
| 1109h | BBC3 | BBC23 | BBC22 | BBC21 | BBC20 | BBC19 | BBC18 | BBC17 | BBC16 |
| 110Ah | BBC4 | BBC31 | BBC30 | BBC29 | BBC28 | BBC27 | BBC26 | BBC25 | BBC24 |
| 110Bh | BEC1 | EC7 | EC6 | EC5 | EC4 | EC3 | EC2 | EC1 | EC0 |
| 110Ch | BEC2 | EC15 | EC14 | EC13 | EC12 | EC11 | EC10 | EC9 | EC8 |
| 110Dh | BEC3 | EC23 | EC22 | EC21 | EC20 | EC19 | EC18 | EC17 | EC16 |
| 110Eh | BLSR | — | BBED | BBCO | BECO | BRA1 | BRA0 | BRLOS | BSYNC |
| 110Fh | BSIM | — | BBED | BBCO | BECO | BRA1 | BRA0 | BRLOS | BSYNC |

9.3 Global Register Definitions

Functions contained in the global registers include: framer reset, LIU reset, device ID, BERT interrupt status, framer interrupt status, IBO configuration, MCLK configuration, and BPCLK configuration. The global registers bit descriptions are presented in this section.

Table 9-10. Global Register Set

| ADDRESS | NAME | DESCRIPTION | R/W |
|---------|-----------------------|--|-----|
| 0F0h | GTCR1 | Global Transceiver Control Register 1 | R/W |
| 0F1h | GFCR | Global Framer Control Register | R/W |
| 0F2h | GTCR2 | Global Transceiver Control Register 2 | R/W |
| 0F3h | GTCCR | Global Transceiver Clock Control Register | R/W |
| 0F4h | — | Reserved | — |
| 0F5h | GLSRR | Global LIU Software Reset Register | R/W |
| 0F6h | GFSRR | Global Framer and BERT Software Reset Register | R/W |
| 0F7h | — | Reserved | — |
| 0F8h | IDR | Device Identification Register | R |
| 0F9h | GFISR | Global Framer Interrupt Status Register | R |
| 0FAh | GBISR | Global BERT Interrupt Status Register | R |
| 0FBh | GLISR | Global LIU Interrupt Status Register | R |
| 0FCh | GFIMR | Global Framers Interrupt Mask Register | R/W |
| 0FDh | GBIMR | Global BERT Interrupt Mask Register | R/W |
| 0FEh | GLIMR | Global LIU Interrupt Mask Register | R/W |
| 01Fh | — | Reserved | — |

Note 1: Reserved registers should only be written with all zeros.

Note 2: The global registers are located in the framer address space. The corresponding address space for the other seven framers is "Reserved," and should be initialized with all zeros for proper operation.

Register Name **GTCR1**
 Register Description: **Global Transceiver Control Register 1**
 Register Address: **0F0h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---------|------|---|-----|------|------|
| Name | — | — | RLOFLTS | GIBO | — | BWE | GCLE | GIPI |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 5: Receive Loss of Frame/Loss of Transmit Clock Indication Select (RLOFLTS).

- 0 = RLOF/LTCx pin indicates framer receive loss of frame
- 1 = RLOF/LTCx pin indicates framer loss of transmit clock

Bit 4: Global IBO Enable (GIBO). This bit is used to select either the internal mux for IBO operation or an external wire-OR operation. Normally this bit should be set = 0 and the internal mux used.

- 0 = Use internal IBO mux
- 1 = Externally wire-OR TSERs and RSERs for IBO operation

Bit 2: Bulk Write Enable (BWE). When this bit is set, a port write to one of the quad ports is mapped into all four ports. This applies to the framer, BERT, and LIU register sets. It must be cleared before performing a read operation. This bit is useful for device initialization.

- 0 = Normal operation
- 1 = Bulk write is enabled

Bit 1: Global Counter Latch Enable (GCLE). A low-to-high transition on this bit will, when enabled, latch the framer performance monitor counters. Each framer can be independently enabled to accept this input. This bit must be cleared and set again to perform another counter latch.

Bit 0: Global Interrupt Pin Inhibit (GIPI).

- 0 = Normal operation. Interrupt pin ($\overline{\text{INTB}}$) will toggle low on an unmasked interrupt condition.
- 1 = Interrupt inhibit. Interrupt pin ($\overline{\text{INTB}}$) is forced high (inactive) when this bit is set.

Register Name: **GFCR**
 Description: **Global Framer Control Register**
 Register Address: **0F1h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|----------|-------|-------|-------|
| Name | IBOMS1 | IBOMS0 | BPCLK1 | BPCLK0 | RFLOSSFS | RFMSS | TCBCS | RCBCS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 and 6: Interleave Bus Operation Mode Select 1 and 0 (IBOMS[1:0]). These bits determine the configuration of the IBO (interleaved bus) multiplexer. These bits should be used in conjunction with the Rx and Tx IBO control registers within each of the framer units. Additional information concerning the IBO multiplexer is given in Section [8.8.2](#).

| IBOMS1 | IBOMS0 | IBO MODE |
|--------|--------|------------------------------|
| 0 | 0 | IBO multiplexer disabled |
| 0 | 1 | 2 devices on bus (4.096MHz) |
| 1 | 0 | 4 devices on bus (8.192MHz) |
| 1 | 1 | 8 devices on bus (16.384MHz) |

Bits 5 and 4: Backplane Clock Select 1 and 0 (BPCLK[1:0]). These bits determine the clock frequency output on the BPCLK pin.

| BPCLK1 | BPCLK0 | BPCLK FREQUENCY |
|--------|--------|-----------------|
| 0 | 0 | 2.048MHz |
| 0 | 1 | 4.096MHz |
| 1 | 0 | 8.192MHz |
| 1 | 1 | 16.384MHz |

Bit 3: Receive Loss of Signal/Signaling Freeze Select (RLOSSFS). This bit controls the function of all four AL/RSIGF/FLOS pins. The receive LOS is further selected between framer LOS and LIU LOS by [GTCR2.2](#).

- 0 = AL/RSIGF/FLOS pin outputs RLOS[1:4] (receive loss)
- 1 = AL/RSIGF/FLOS pin outputs RSIGF[1:4] (receive-signaling freeze)

Bit 2: Receive Frame/Multiframe Sync Select (RFMSS). This bit controls the function of all four RMSYNC/RFSYNC pins.

- 0 = RMSYNC/RFSYNC pin outputs RFSYNC[1:4] (receive frame sync)
- 1 = RMSYNC/RFSYNC pin outputs RMSYNC[1:4] (receive multiframe sync)

Bit 1: Transmit Channel Block/Clock Select (TCBCS). This bit controls the function of all four TCHBLK/CLK pins.

- 0 = TCHBLK/CLK pin outputs TCHBLK[1:4] (transmit channel block)
- 1 = TCHBLK/CLK pin outputs TCHCLK[1:4] (transmit channel clock)

Bit 0: Receive Channel Block/Clock Select (RCBCS). This bit controls the function of all four RCHBLK/CLK pins.

- 0 = RCHBLK/CLK pin outputs RCHBLK[1:4] (receive channel block)
- 1 = RCHBLK/CLK pin outputs RCHCLK[1:4] (receive channel clock)

Register Name: **GTCR2**
 Register Description: **Global Transceiver Control Register 2**
 Register Address: **0F2h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|------|-------------|---|
| Name | — | — | — | — | — | LOSS | TSSYNCEOSEL | — |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 2: LOS Selection (LOSS). If this bit is set, the AL/RSIGF/FLOS pins can be driven with LIU loss. If reset, they are driven by framer LOS. The selection of whether to drive AL/RSIGF/FLOS pins with LOS (analog or digital) or signalling freeze is controlled by [GFCR.2](#). This selection affects all ports.

Bit 1: Transmit System Synchronization I/O Select (TSSYNCEOSEL). If this bit is set to a 1, the TSSYNCEO is an 8kHz output synchronous to the BPCLK. This “frame pulse” can be used in conjunction with the backplane clock to provide IBO signals for a system backplane. If this bit is reset, TSSYNCEO is an input. An 8kHz frame pulse is required for transmit synchronization and IBO operation.

Register Name: **GTCCR**
 Register Description: **Global Transceiver Clock Control Register**
 Register Address: **0F3h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----------|-----------|-----------|-----------|----------|---------|------|------|
| Name | BPREFSEL3 | BPREFSEL2 | BPREFSEL1 | BPREFSEL0 | BFREQSEL | FREQSEL | MPS1 | MPS0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 4: Backplane Clock Reference Selects (BPREFSEL[3:0]). These bits select which reference clock source will be used for BPCLK generation. The BPCLK can be generated from the LIU recovered clock, an external reference, or derivatives of MCLK input. This is shown in [Table 9-11](#). See [Figure 8-1](#) for additional information.

Bit 3: Backplane Frequency Select (BFREQSEL). In conjunction with BPRFSEL[3:0], this bit identifies the reference clock frequency used by the DS26524 backplane clock generation circuit. Note that the setting of this bit should match the T1E1 selection for the LIU whose recovered clock is being used to generate the backplane clock. See [Figure 8-1](#) for additional information.

- 0 = Backplane reference clock is 2.048MHz.
- 1 = Backplane reference clock is 1.544MHz.

Bit 2: Frequency Selection (FREQSEL). In conjunction with the MPS[1:0] bits, this bit selects the external MCLK frequency of the signal input at the MCLK pin of the DS26524.

- 0 = The external master clock is 2.048MHz or multiple thereof.
- 1 = The external master clock is 1.544MHz or multiple thereof.

Bits 1 and 0: Master Period Select 1 and 0 (MPS[1:0]). In conjunction with the FREQSEL bit, these bits select the external MCLK frequency of the signal input at the MCLK pin of the DS26524. This is shown in [Table 9-12](#).

Table 9-11. Backplane Reference Clock Select

| BPREFSEL3 | BPREFSEL2 | BPREFSEL1 | BPREFSEL0 | BFREQSEL | REFERENCE CLOCK SOURCE |
|-----------|-----------|-----------|-----------|----------|---|
| 0 | 0 | 0 | 0 | 0 | 2.048MHz RCLK1 |
| 0 | 0 | 0 | 0 | 1 | 1.544MHz RCLK1 |
| 0 | 0 | 0 | 1 | 0 | 2.048MHz RCLK2 |
| 0 | 0 | 0 | 1 | 1 | 1.544MHz RCLK2 |
| 0 | 0 | 1 | 0 | 0 | 2.048MHz RCLK3 |
| 0 | 0 | 1 | 0 | 1 | 1.544MHz RCLK3 |
| 0 | 0 | 1 | 1 | 0 | 2.048MHz RCLK4 |
| 0 | 0 | 1 | 1 | 1 | 1.544MHz RCLK4 |
| 1 | 0 | 0 | 0 | 1 | 1.544MHz derived from MCLK. (REFCLKIO is an output.) |
| 1 | 0 | 0 | 1 | 0 | 2.048MHz derived from MCLK. (REFCLKIO is an output.) |
| 1 | 0 | 1 | 0 | 0 | 2.048MHz external clock input at REFCLKIO. (REFCLKIO is an input.) |
| 1 | 0 | 1 | 0 | 1 | 1.544MHz external clock input at REFCLKIO. (REFCLKIO is an input.) |

Table 9-12. Master Clock Input Selection

| FREQSEL | MPS1 | MPS0 | MCLK (MHz \pm50ppm) |
|----------------|-------------|-------------|---|
| 0 | 0 | 0 | 2.048 |
| 0 | 0 | 1 | 4.096 |
| 0 | 1 | 0 | 8.192 |
| 0 | 1 | 1 | 16.384 |
| 1 | 0 | 0 | 1.544 |
| 1 | 0 | 1 | 3.088 |
| 1 | 1 | 0 | 6.176 |
| 1 | 1 | 1 | 12.352 |

Register Name: **GLSRR**
 Register Description: **Global LIU Software Reset Register**
 Register Address: **0F5h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|--------|--------|--------|--------|
| Name | — | — | — | — | LSRST4 | LSRST3 | LSRST2 | LSRST1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 3: Channel 4 LIU Software Reset (LSRST4). LIU logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.

0 = Normal operation
 1 = Reset LIU

Bit 2: Channel 3 LIU Software Reset (LSRST3). LIU logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.

0 = Normal operation
 1 = Reset LIU

Bit 1: Channel 2 LIU Software Reset (LSRST2). LIU logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.

0 = Normal operation
 1 = Reset LIU

Bit 0: Channel 1 LIU Software Reset (LSRST1). LIU logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.

0 = Normal operation
 1 = Reset LIU

Register Name: **GFSRR**
 Register Description: **Global Framer and BERT Software Reset Register**
 Register Address: **0F6h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|--------|--------|--------|--------|
| Name | — | — | — | — | FSRST4 | FSRST3 | FSRST2 | FSRST1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 3: Channel 4 Framer and BERT Software Reset (FSRST4). Framer logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.

0 = Normal operation

1 = Reset framer and BERT

Bit 2: Channel 3 Framer and BERT Software Reset (FSRST3). Framer logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.

0 = Normal operation

1 = Reset framer and BERT

Bit 1: Channel 2 Framer and BERT Software Reset (FSRST2). Framer logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.

0 = Normal operation

1 = Reset framer and BERT

Bit 0: Channel 1 Framer and BERT Software Reset (FSRST1). Framer logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.

0 = Normal operation

1 = Reset framer and BERT

Register Name: **IDR**
 Register Description: **Device Identification Register**
 Register Address: **0F8h**

| | | | | | | | | |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
| Default | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

Bits 7 to 3: Device ID (ID[7:3]). The upper five bits of the IDR are used to display the DS26524 ID.

Table 9-13. Device ID Codes in this Product Family

| DEVICE | ID7 | ID6 | ID5 | ID4 | ID3 |
|---------|-----|-----|-----|-----|-----|
| DS26528 | 0 | 1 | 0 | 1 | 1 |
| DS26524 | 0 | 1 | 1 | 0 | 0 |
| DS26522 | 0 | 1 | 1 | 0 | 1 |
| DS26521 | 0 | 1 | 1 | 1 | 0 |

Bits 2 to 0: Silicon Revision Bits (ID[2:0]). The lower three bits of the IDR are used to display a sequential number denoting the die revision of the chip. The initial silicon revision = "000," and is incremented with each silicon revision. This value is not the same as the two-character device revision on the top brand of the device. This is due to the fact that portions of the device assembly other than the silicon may change, causing the device revision increment on the brand without having a revision of the silicon. ID0 is the LSB of a decimal code that represents the chip revision.

Register Name: **GFISR**
 Register Description: **Global Framer Interrupt Status Register**
 Register Address: **0F9h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|------|------|------|------|
| Name | — | — | — | — | FIS4 | FIS3 | FIS2 | FIS1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The GFISR register reports the framer interrupt status for each of the four T1/E1 framers. A logic one in the associated bit location indicates a framer has set its interrupt signal.

Bit 3: Framer Interrupt Status 4 (FIS4).

0 = Framer 4 has not issued an interrupt.

1 = Framer 4 has issued an interrupt.

Bit 0: Framer Interrupt Status 3 (FIS3).

0 = Framer 3 has not issued an interrupt.

1 = Framer 3 has issued an interrupt.

Bit 0: Framer Interrupt Status 2 (FIS2).

0 = Framer 2 has not issued an interrupt.

1 = Framer 2 has issued an interrupt.

Bit 0: Framer Interrupt Status 1 (FIS1).

0 = Framer 1 has not issued an interrupt.

1 = Framer 1 has issued an interrupt.

Register Name: **GBISR**
 Register Description: **Global BERT Interrupt Status Register**
 Register Address: **0FAh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|------|------|------|------|
| Name | — | — | — | — | BIS4 | BIS3 | BIS2 | BIS1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The GBISR register reports the interrupt status for each of the four T1/E1 bit error-rate testers (BERTs). A logic one in the associated bit location indicates a BERT has set its interrupt signal.

Bit 3: BERT Interrupt Status 4 (BIS4).

0 = BERT 4 has not issued an interrupt.

1 = BERT 4 has issued an interrupt.

Bit 2: BERT Interrupt Status 3 (BIS3).

0 = BERT 3 has not issued an interrupt.

1 = BERT 3 has issued an interrupt.

Bit 1: BERT Interrupt Status 2 (BIS2).

0 = BERT 2 has not issued an interrupt.

1 = BERT 2 has issued an interrupt.

Bit 0: BERT Interrupt Status 1 (BIS1).

0 = BERT 1 has not issued an interrupt.

1 = BERT 1 has issued an interrupt.

Register Name: **GLISR**
 Register Description: **Global LIU Interrupt Status Register**
 Register Address: **0FBh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|------|------|------|------|
| Name | — | — | — | — | LIS4 | LIS3 | LIS2 | LIS1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The GLISR register reports the LIU interrupt status for each of the four T1/E1 LIUs. A logic one in the associated bit location indicates a LIU has set its interrupt signal.

Bit 3: LIU Interrupt Status 4 (LIS4).

0 = LIU 4 has not issued an interrupt.

1 = LIU 4 has issued an interrupt.

Bit 2: LIU Interrupt Status 3 (LIS3).

0 = LIU 3 has not issued an interrupt.

1 = LIU 3 has issued an interrupt.

Bit 1: LIU Interrupt Status 2 (LIS2).

0 = LIU 2 has not issued an interrupt.

1 = LIU 2 has issued an interrupt.

Bit 0: LIU Interrupt Status 1 (LIS1).

0 = LIU 1 has not issued an interrupt.

1 = LIU 1 has issued an interrupt.

Register Name: **GFIMR**
 Register Description: **Global Framer Interrupt Mask Register**
 Register Address: **0FCh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|------|------|------|------|
| Name | — | — | — | — | FIM4 | FIM3 | FIM2 | FIM1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 3: Framer 4 Interrupt Mask (FIM4).

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 2: Framer 3 Interrupt Mask (FIM3).

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 1: Framer 2 Interrupt Mask (FIM2).

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 0: Framer 1 Interrupt Mask (FIM1).

0 = Interrupt masked.
 1 = Interrupt enabled.

Register Name: **GBIMR**
 Register Description: **Global BERT Interrupt Mask Register**
 Register Address: **0FDh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|------|------|------|------|
| Name | — | — | — | — | BIM4 | BIM3 | BIM2 | BIM1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 3: BERT Interrupt Mask 4 (BIM4).

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 2: BERT Interrupt Mask 3 (BIM3).

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 1: BERT Interrupt Mask 2 (BIM2).

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 0: BERT Interrupt Mask 1 (BIM1).

0 = Interrupt masked.
 1 = Interrupt enabled.

Register Name: **GLIMR**
 Register Description: **Global LIU Interrupt Mask Register**
 Register Address: **0FEh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|------|------|------|------|
| Name | — | — | — | — | LIM4 | LIM3 | LIM2 | LIM1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 3: LIU Interrupt Mask 4 (LIM4).

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 2: LIU Interrupt Mask 3 (LIM3).

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 1: LIU Interrupt Mask 2 (LIM2).

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 0: LIU Interrupt Mask 1 (LIM1).

0 = Interrupt masked.
 1 = Interrupt enabled.

9.4 Framer Register Definitions

See [Table 9-3](#) for the complete framer register list.

9.4.1 Receive Register Definitions

Register Name: **RHC**
 Register Description: **Receive HDLC Control Register**
 Register Address: **010h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-----|------|-------|-------|-------|-------|-------|
| Name | RCRCD | RHR | RHMS | RHCS4 | RHCS3 | RHCS2 | RHCS1 | RHCS0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive CRC-16 Display (RCRCD).

- 0 = Do not write received CRC-16 code to FIFO (default)
- 1 = Write received CRC-16 code to FIFO after last octet of packet

Bit 6: Receive HDLC Reset (RHR). Will reset the receive HDLC controller and flush the receive FIFO. Note that this bit is a acknowledged reset. The host should set this bit and the DS26524 will clear it once the reset operation is complete. The DS26524 will complete the HDLC reset within two frames.

- 0 = Normal operation
- 1 = Reset receive HDLC controller and flush the receive FIFO

Bit 5: Receive HDLC Mapping Select (RHMS).

- 0 = Receive HDLC assigned to channels
- 1 = Receive HDLC assigned to FDL (T1 mode), Sa bits (E1 mode)

Bit 4 to 0: Receive HDLC Channel Select 4 to 0 (RHCS[4:0]). These bits determine which DS0 is mapped to the HDLC controller when enabled with RHMS = 0. RHCS[4:0] = all 0s selects channel 1, RHCS[4:0] = all 1s selects channel 32 (E1). A change to the receive HDLC channel select is acknowledged only after a receive HDLC reset (RHR).

Register Name: **RHBSE**
 Register Description: **Receive HDLC Bit Suppress Register**
 Register Address: **011h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | BSE8 | BSE7 | BSE6 | BSE5 | BSE4 | BSE3 | BSE2 | BSE1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive Channel Bit 8 Suppress (BSE8). MSB of the channel. Set to one to stop this bit from being used.

Bit 6: Receive Channel Bit 7 Suppress (BSE7). Set to one to stop this bit from being used.

Bit 5: Receive Channel Bit 6 Suppress (BSE6). Set to one to stop this bit from being used.

Bit 4: Receive Channel Bit 5 Suppress (BSE5). Set to one to stop this bit from being used.

Bit 3: Receive Channel Bit 4 Suppress (BSE4). Set to one to stop this bit from being used.

Bit 2: Receive Channel Bit 3 Suppress (BSE3). Set to one to stop this bit from being used.

Bit 1: Receive Channel Bit 2 Suppress (BSE2). Set to one to stop this bit from being used.

Bit 0: Receive Channel Bit 1 Suppress (BSE1). LSB of the channel. Set to one to stop this bit from being used.

Register Name: **RDS0SEL**
 Register Description: **Receive Channel Monitor Select Register**
 Register Address: **012h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|------|------|------|------|------|
| Name | — | — | — | RCM4 | RCM3 | RCM2 | RCM1 | RCM0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 4 to 0: Receive Channel Monitor Bits (RCM[4:0]). RCM0 is the LSB of a 5-bit channel select that determines which receive DS0 channel data will appear in the RDS0M register.

Register Name: **RSIGC**
 Register Description: **Receive-Signaling Control Register**
 Register Address: **013h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|-------|---|------|------|------|
| Name | — | — | — | RFSA1 | — | RSFF | RSFE | RSIE |
| | — | — | — | CASMS | — | RSFF | RSFE | RSIE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 4 (T1 Mode): Receive Force Signaling All Ones (RFSA1).

0 = do not force robbed bit signaling to all ones

1 = force signaling bits to all ones on a per-channel basis according to the [T1RSAOI1:T1RSAOI3](#) registers.

Bit 4 (E1 Mode): CAS Mode Select (CASMS).

0 = The DS26524 will initiate a resync when two consecutive multiframe alignment signals have been received with an error.

1 = The DS26524 will initiate a resync when two consecutive multiframe alignment signals have been received with an error, or 1 multiframe has been received with all the bits in time slot 16 in state 0.

Alignment criteria is met when at least one bit in state 1 is present in the time slot 16 preceding the multiframe alignment signal first detected (G.732 alternate criteria).

Bit 2: Receive-Signaling Force Freeze (RSFF). Freezes receive-side signaling at RSIG (and RSER if receive-signaling reinsertion is enabled); will override receive freeze enable (RFE).

0 = do not force a freeze event

1 = force a freeze event

Bit 1: Receive-Signaling Freeze Enable (RSFE).

0 = no freezing of receive-signaling data will occur

1 = allow freezing of receive-signaling data at RSIG (and RSER if receive-signaling reinsertion is enabled)

Bit 0: Receive-Signaling Integration Enable (RSIE).

0 = signaling changes of state reported on any change in selected channels

1 = signaling must be stable for three multiframes in order for a change of state to be reported

Register Name: **T1RCR2 (T1 Mode)**
 Register Description: **Receive Control Register 2**
 Register Address: **014h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| | | | | | | | | |
|---------|---|---|---|--------|------|------|-------|-------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | — | — | RSLC96 | OOF2 | OOF1 | RAIIE | RD4RM |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 4: Receive SLC-96 Synchronizer Enable (RSLC96). See Section [8.9.4.5](#) for SLC-96 details.

0 = SLC-96 synchronizer is disabled

1 = SLC-96 synchronizer is enabled

Bits 3 and 2: Out of Frame Select Bits (OOF[2:1]).

| OOF2 | OOF1 | OUT OF FRAME CRITERIA |
|------|------|-------------------------|
| 0 | 0 | 2/4 frame bits in error |
| 0 | 1 | 2/5 frame bits in error |
| 1 | 0 | 2/6 frame bits in error |
| 1 | 1 | 2/6 frame bits in error |

Bit 1: Receive RAI Integration Enable (RAIIE). The ESF RAI indication can be interrupted for a period not to exceed 100ms per interruption (T1.403). In ESF mode, setting RAIIE will cause the RAI status from the DS26524 to be integrated for 200ms.

0 = RAI detects when 16 consecutive patterns of 00FF appear in the FDL.

RAI clears when 14 or fewer patterns of 00FF hex out of 16 possible appear in the FDL.

1 = RAI detects when the condition has been present for greater than 200ms.

RAI clears when the condition has been absent for greater than 200ms.

Bit 0: Receive-Side D4 Remote Alarm Select (RD4RM).

0 = zeros in bit 2 of all channels

1 = a one in the S-bit position of frame 12 (J1 Yellow Alarm Mode)

Register Name: **E1RSAIMR (E1 Mode Only)**
 Register Description: **Receive Sa-Bit Interrupt Mask Register**
 Register Address: **014h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|--------|--------|--------|--------|--------|
| Name | — | — | — | RSa4IM | RSa5IM | RSa6IM | RSa7IM | RSa8IM |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 4: Sa4 Change Detect Interrupt Mask (RSa4IM). This bit will enable the change detect interrupt for the Sa4 bits. Any change of state of the Sa4 bit will then generate an interrupt in [RLS7.0](#) to indicate the change of state.

0 = interrupt masked
 1 = interrupt enabled

Bit 3: Sa5 Change Detect Interrupt Mask (RSa5IM). This bit will enable the change detect interrupt for the Sa5 bits. Any change of state of the Sa5 bit will then generate an interrupt in [RLS7.0](#) to indicate the change of state.

0 = interrupt masked
 1 = interrupt enabled

Bit 2: Sa6 Change Detect Interrupt Mask (RSa6IM). This bit will enable the change detect interrupt for the Sa6 bits. Any change of state of the Sa6 bit will then generate an interrupt in [RLS7.0](#) to indicate the change of state.

0 = interrupt masked
 1 = interrupt enabled

Bit 1: Sa7 Change Detect Interrupt Mask (RSa7IM). This bit will enable the change detect interrupt for the Sa7 bits. Any change of state of the Sa7 bit will then generate an interrupt in [RLS7.0](#) to indicate the change of state.

0 = interrupt masked
 1 = interrupt enabled

Bit 0: Sa8 Change Detect Interrupt Mask (RSa8IM). This bit will enable the change detect interrupt for the Sa8 bits. Any change of state of the Sa8 bit will then generate an interrupt in [RLS7.0](#) to indicate the change of state.

0 = interrupt masked
 1 = interrupt enabled

Register Name: **T1RBOCC (T1 Mode Only)**
 Register Description: **Receive BOC Control Register**
 Register Address: **015h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|---|------|------|---|------|------|---|
| Name | RBR | — | RBD1 | RBD0 | — | RBF1 | RBF0 | — |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive BOC Reset (RBR). The host should set this bit to force a reset of the BOC circuitry. Note that this is an acknowledged reset, that is, the host need only set the bit and the DS26524 will clear it once the reset operation is complete (less than 250µs). Modifications to the RBF[1:0] and RBD[1:0] bits will not be applied to the BOC controller until a BOC reset has been completed.

Bits 5 and 4: Receive BOC Disintegration Bits (RBD[1:0]). The BOC disintegration filter sets the number of message bits that must be received without a valid BOC to set the BC bit indicating that a valid BOC is no longer being received.

| RBD1 | RBD0 | CONSECUTIVE MESSAGE BITS FOR BOC CLEAR IDENTIFICATION |
|------|------|---|
| 0 | 0 | 16 |
| 0 | 1 | 32 |
| 1 | 0 | 48 |
| 1 | 1 | 64 (See Note 1) |

Bits 2 and 1: Receive BOC Filter Bits (RBF[1:0]). The BOC filter sets the number of consecutive patterns that must be received without error prior to an indication of a valid message.

| RBF1 | RBF0 | CONSECUTIVE BOC CODES FOR VALID SEQUENCE IDENTIFICATION |
|------|------|---|
| 0 | 0 | None |
| 0 | 1 | 3 |
| 1 | 0 | 5 |
| 1 | 1 | 7 (See Note 1) |

Note 1: The DS26524's BOC controller does not integrate and disintegrate concurrently. Therefore, if the maximum integration time and the maximum disintegration time are used together, BOC messages that repeat fewer than 11 times may not be detected.

Register Name: **RIDR1 to RIDR32**
 Register Description: **Receive Idle Code Definition Registers 1 to 32**
 Register Address: **020h to 03Fh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Per-Channel Idle Code Bits (C[7:0]). C0 is the LSB of the code (this bit is transmitted last). Address 020h is for channel 1. Address 037h is for channel 24. Address 03Fh is for channel 32. RIDR1:RIDR24 are T1 mode only. RIDR25:RIDR32 are E1 mode only.

Register Name: **T1RSAOI1, T1RSAOI2, T1RSAOI3 (T1 Mode Only)**
 Register Description: **Receive-Signaling All-Ones Insertion Registers 1 to 3**
 Register Address: **038h, 039h, 03Ah + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | (MSB) 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) | |
|---------|---------|------|------|------|------|------|------|---------|----------|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | T1RSAOI1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | T1RSAOI2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | T1RSAOI3 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Setting any of the CH[1:24] bits in the T1RSAOI1:T1RSAOI3 registers will cause signaling data to be replaced with logic ones as reported on RSER. The RSIG signal will continue to report received signaling data. Note that this feature must be enabled with control bit [RSIGC.4](#).

Register Name: **T1RDMWE1, T1RDMWE2, T1RDMWE3 (T1 Mode Only)**
 Register Description: **T1 Receive Digital Milliwatt Enable Registers 1 to 3**
 Register Address: **03Ch, 03Dh, 03Eh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | (MSB) 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) | |
|---------|---------|------|------|------|------|------|------|---------|----------|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | T1RDMWE1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | T1RDMWE2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | T1RDMWE3 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Bits 7 to 0: Receive Digital Milliwatt Enable for Channels 1 to 24 (CH[1:24]).

0 =do not affect the receive data associated with this channel

1 = replace the receive data associated with this channel with digital milliwatt code

Register Name: **RS1 to RS16**
 Register Description: **Receive-Signaling Registers 1 to 16**
 Register Address: **040h to 04Fh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

T1 Mode:
(MSB)

| | | | | (LSB) | | | | |
|--------|--------|--------|--------|--------------|--------|--------|--------|-------------|
| CH1-A | CH1-B | CH1-C | CH1-D | CH13-A | CH13-B | CH13-C | CH13-D | RS1 |
| CH2-A | CH2-B | CH2-C | CH2-D | CH14-A | CH14-B | CH14-C | CH14-D | RS2 |
| CH3-A | CH3-B | CH3-C | CH3-D | CH15-A | CH15-B | CH15-C | CH15-D | RS3 |
| CH4-A | CH4-B | CH4-C | CH4-D | CH16-A | CH16-B | CH16-C | CH16-D | RS4 |
| CH5-A | CH5-B | CH5-C | CH5-D | CH17-A | CH17-B | CH17-C | CH17-D | RS5 |
| CH6-A | CH6-B | CH6-C | CH6-D | CH18-A | CH18-B | CH18-C | CH18-D | RS6 |
| CH7-A | CH7-B | CH7-C | CH7-D | CH19-A | CH19-B | CH19-C | CH19-D | RS7 |
| CH8-A | CH8-B | CH8-C | CH8-D | CH20-A | CH20-B | CH20-C | CH20-D | RS8 |
| CH9-A | CH9-B | CH9-C | CH9-D | CH21-A | CH21-B | CH21-C | CH21-D | RS9 |
| CH10-A | CH10-B | CH10-C | CH10-D | CH22-A | CH22-B | CH22-C | CH22-D | RS10 |
| CH11-A | CH11-B | CH11-C | CH11-D | CH23-A | CH23-B | CH23-C | CH23-D | RS11 |
| CH12-A | CH12-B | CH12-C | CH12-D | CH24-A | CH24-B | CH24-C | CH24-D | RS12 |

E1 Mode:
(MSB)

| | | | | (LSB) | | | | |
|--------|--------|--------|--------|--------------|--------|--------|--------|-------------|
| 0 | 0 | 0 | 0 | X | Y | X | X | RS1 |
| CH1-A | CH1-B | CH1-C | CH1-D | CH16-A | CH16-B | CH16-C | CH16-D | RS2 |
| CH2-A | CH2-B | CH2-C | CH2-D | CH17-A | CH17-B | CH17-C | CH17-D | RS3 |
| CH3-A | CH3-B | CH3-C | CH3-D | CH18-A | CH18-B | CH18-C | CH18-D | RS4 |
| CH4-A | CH4-B | CH4-C | CH4-D | CH19-A | CH19-B | CH19-C | CH19-D | RS5 |
| CH5-A | CH5-B | CH5-C | CH5-D | CH20-A | CH20-B | CH20-C | CH20-D | RS6 |
| CH6-A | CH6-B | CH6-C | CH6-D | CH21-A | CH21-B | CH21-C | CH21-D | RS7 |
| CH7-A | CH7-B | CH7-C | CH7-D | CH22-A | CH22-B | CH22-C | CH22-D | RS8 |
| CH8-A | CH8-B | CH8-C | CH8-D | CH23-A | CH23-B | CH23-C | CH23-D | RS9 |
| CH9-A | CH9-B | CH9-C | CH9-D | CH24-A | CH24-B | CH24-C | CH24-D | RS10 |
| CH10-A | CH10-B | CH10-C | CH10-D | CH25-A | CH25-B | CH25-C | CH25-D | RS11 |
| CH11-A | CH11-B | CH11-C | CH11-D | CH26-A | CH26-B | CH26-C | CH26-D | RS12 |
| CH12-A | CH12-B | CH12-C | CH12-D | CH27-A | CH27-B | CH27-C | CH27-D | RS13 |
| CH13-A | CH13-B | CH13-C | CH13-D | CH28-A | CH28-B | CH28-C | CH28-D | RS14 |
| CH14-A | CH14-B | CH14-C | CH14-D | CH29-A | CH29-B | CH29-C | CH29-D | RS15 |
| CH15-A | CH15-B | CH15-C | CH15-D | CH30-A | CH30-B | CH30-C | CH30-D | RS16 |

In the ESF framing mode, there can be up to four signaling bits per channel (A, B, C, and D). In the D4 framing mode, there are only two signaling bits per channel (A and B). In the D4 framing mode, the framer will repeat the A and B signaling data in the C and D bit locations. Therefore, when the framer is operated in D4 framing mode, the user will need to retrieve the signaling bits every 1.5ms as opposed to 3ms for ESF mode. The receive-signaling registers are frozen and not updated during a loss of sync condition. They will contain the most recent signaling information before the "OOF" occurred.

Register Name: **LCVCR1**
 Register Description: **Line Code Violation Count Register 1**
 Register Address: **050h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|-------|-------|
| Name | LCVC15 | LCVC14 | LCVC13 | LCVC12 | LCVC11 | LCVC10 | LCVC9 | LCVC8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Line Code Violation Counter Bits 15 to 8 (LCVC[15:8]). LCVC15 is the MSB of the 16-bit code violation count.

Register Name: **LCVCR2**
 Register Description: **Line Code Violation Count Register 2**
 Register Address: **051h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | LCVC7 | LCVC6 | LCVC5 | LCVC4 | LCVC3 | LCVC2 | LCVC1 | LCVC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Line Code Violation Counter Bits 7 to 0 (LCVC[7:0]). LCVC0 is the LSB of the 16-bit code violation count.

Register Name: **PCVCR1**
 Register Description: **Path Code Violation Count Register 1**
 Register Address: **052h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|-------|-------|
| Name | PCVC15 | PCVC14 | PCVC13 | PCVC12 | PCVC11 | PCVC10 | PCVC9 | PCVC8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Path Code Violation Counter Bits 15 to 8 (PCVC[15:8]). PCVC15 is the MSB of the 16-bit path code violation count.

Register Name: **PCVCR2**
 Register Description: **Path Code Violation Count Register 2**
 Register Address: **053h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | PCVC7 | PCVC6 | PCVC5 | PCVC4 | PCVC3 | PCVC2 | PCVC1 | PCVC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Path Code Violation Counter Bits 0 to 7 (PCVC[7:0]). PCVC0 is the LSB of the 16-bit path code violation count.

Register Name: **FOSCR1**
 Register Description: **Frames Out of Sync Count Register 1**
 Register Address: **054h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|------|------|
| Name | FOS15 | FOS14 | FOS13 | FOS12 | FOS11 | FOS10 | FOS9 | FOS8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Frames Out of Sync Counter Bits 15 to 8 (FOS[15:8]). FOS15 is the MSB of the 16-bit frames out of sync count.

Register Name: **FOSCR2**
 Register Description: **Frames Out of Sync Count Register 2**
 Register Address: **055h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | FOS7 | FOS6 | FOS5 | FOS4 | FOS3 | FOS2 | FOS1 | FOS0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Frames Out of Sync Counter Bits 7 to 0 (FOS[7:0]). FOS0 is the LSB of the 16-bit frames out of sync count.

Register Name: **E1EBCR1 (E1 Mode Only)**
 Register Description: **E-Bit Count Register 1**
 Register Address: **056h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|-----|-----|
| Name | EB15 | EB14 | EB13 | EB12 | EB11 | EB10 | EB9 | EB8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: E-Bit Counter Bits 15 to 8 (EB[15:8]). EB15 is the MSB of the 16-bit E-bit count.

Register Name: **E1EBCR2 (E1 Mode Only)**
 Register Description: **E-Bit Count Register 2**
 Register Address: **057h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | EB7 | EB6 | EB5 | EB4 | EB3 | EB2 | EB1 | EB0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: E-Bit Counter Bits 7 to 0 (EB[7:0]). EB0 is the LSB of the 16-bit E-bit count.

Register Name: **RDS0M**
 Register Description: **Receive DS0 Monitor Register**
 Register Address: **060h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive DS0 Channel Bits (B[1:8]). Receive channel data that has been selected by the Receive Channel Monitor Select register ([RDS0SEL](#)). B8 is the LSB of the DS0 channel (last bit to be received).

Register Name: **E1RFRID (E1 Mode Only)**
 Register Description: **Receive Firmware Revision ID Register**
 Register Address: **061h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | FR7 | FR6 | FR5 | FR4 | FR3 | FR2 | FR1 | FR0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Firmware Revision (FR[7:0]). This read-only register reports the current revision of the receive firmware.

Register Name: **T1RFDL (T1 Mode)**
 Register Description: **Receive FDL Register**
 Register Address: **062h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | RFDL7 | RFDL6 | RFDL5 | RFDL4 | RFDL3 | RFDL2 | RFDL1 | RFDL0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: This register has an alternate definition for E1 mode. See [E1RRTS7](#).

Bit 7: Receive FDL Bit 7 (RFDL7). MSB of the received FDL code.

Bit 6: Receive FDL Bit 6 (RFDL6).

Bit 5: Receive FDL Bit 5 (RFDL5).

Bit 4: Receive FDL Bit 4 (RFDL4).

Bit 3: Receive FDL Bit 3 (RFDL3).

Bit 2: Receive FDL Bit 2 (RFDL2).

Bit 1: Receive FDL Bit 1 (RFDL1).

Bit 0: Receive FDL Bit 0 (RFDL0). LSB of the received FDL code.

Register Name: **E1RRTS7 (E1 Mode)**
 Register Description: **Receive Real-Time Status Register 7**
 Register Address: **062h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|--------|-------|-------|
| Name | CSC5 | CSC4 | CSC3 | CSC2 | CSC0 | CRC4SA | CASSA | FASSA |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: This register has an alternate definition for T1 mode. See [T1RFDL](#). All bits in this register are real-time (not latched).

Bits 7 to 3: CRC-4 Sync Counter Bits (CSC[5:2] and CSC0). The CRC-4 sync counter increments each time the 8ms CRC-4 multiframe search times out. The counter is cleared when the framer has successfully obtained synchronization at the CRC-4 level. The counter can also be cleared by disabling the CRC-4 mode ([RCR1.3](#) = 0). This counter is useful for determining the amount of time the framer has been searching for synchronization at the CRC-4 level. ITU-T G.706 suggests that if synchronization at the CRC-4 level cannot be obtained within 400ms, then the search should be abandoned and proper action taken. The CRC-4 sync counter will saturate (not rollover). CSC0 is the LSB of the 6-bit counter. (CSC1 is omitted to allow resolution to > 400ms using 5 bits.)

Bit 2: CRC-4 MF Sync Active (CRC4SA). Set while the synchronizer is searching for the CRC-4 MF alignment word.

Bit 1: CAS MF Sync Active (CASSA). Set while the synchronizer is searching for the CAS MF alignment word.

Bit 0: FAS Sync Active (FASSA). Set while the synchronizer is searching for alignment at the FAS level.

Register Name: **T1RBOC (T1 Mode)**
 Register Description: **Receive BOC Register**
 Register Address: **063h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|-------|-------|-------|-------|-------|-------|
| Name | — | — | RBOC5 | RBOC4 | RBOC3 | RBOC2 | RBOC1 | RBOC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 5: BOC Bit 5 (RBOC5).

Bit 4: BOC Bit 4 (RBOC4).

Bit 3: BOC Bit 3 (RBOC3).

Bit 2: BOC Bit 2 (RBOC2).

Bit 1: BOC Bit 1 (RBOC1).

Bit 0: BOC Bit 0 (RBOC0).

The T1RBOC register always contains the last valid BOC received. The Receive FDL register ([T1RFDL](#)) reports the incoming Facility Data Link (FDL) or the incoming Fs bits. The LSB is received first. In D4 framing mode, RFDL updates on multiframe boundaries and reports the six Fs bits in RFDL[5:0].

Register Name: **T1RSLC1, T1RSLC2, T1RSLC3 (T1 Mode)**
 Register Description: **Receive SLC-96 Data Link Registers 1 to 3**
 Register Address: **064h, 065h, 066h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | (MSB) 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) | |
|---------|---------|----|-----|-----|-----|-----|-----|---------|---------|
| Name | C8 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | T1RSLC1 |
| | M2 | M1 | S=0 | S=1 | S=0 | C11 | C10 | C9 | T1RSLC2 |
| | S=1 | S4 | S3 | S2 | S1 | A2 | A1 | M3 | T1RSLC3 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Note: These registers have an alternate definition for E1 mode. See [E1RAF](#), [E1RNAF](#), and [E1RSIAF](#).

Register Name: **E1RAF (E1 Mode)**
 Register Description: **E1 Receive Align Frame Register**
 Register Address: **064h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|---|---|---|---|---|---|---|
| Name | Si | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: This register has an alternate definition for T1 mode. See [T1RSLC1](#).

Bit 7: International Bit (Si).

Bit 6: Frame Alignment Signal Bit (0).

Bit 5: Frame Alignment Signal Bit (0).

Bit 4: Frame Alignment Signal Bit (1).

Bit 3: Frame Alignment Signal Bit (1).

Bit 2: Frame Alignment Signal Bit (0).

Bit 1: Frame Alignment Signal Bit (1).

Bit 0: Frame Alignment Signal Bit (1).

Register Name: **E1RNAF (E1 Mode)**
 Register Description: **E1 Receive Non-Align Frame Register**
 Register Address: **065h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|---|---|-----|-----|-----|-----|-----|
| Name | Si | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: This register has an alternate definition for T1 mode. See [T1RSLC2](#).

Bit 7: International Bit (Si).

Bit 6: Frame Non-Alignment Signal Bit (1).

Bit 5: Remote Alarm (A).

Bit 4: Additional Bit 4 (Sa4).

Bit 3: Additional Bit 5 (Sa5).

Bit 2: Additional Bit 6 (Sa6).

Bit 1: Additional Bit 7 (Sa7).

Bit 0: Additional Bit 8 (Sa8).

Register Name: **E1RSiAF (E1 Mode)**
 Register Description: **E1 Received Si Bits of the Align Frame Register**
 Register Address: **066h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|------|------|------|------|------|
| Name | SiF14 | SiF12 | SiF10 | SiF8 | SiF6 | SiF4 | SiF2 | SiF0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: This register has an alternate definition for T1 mode. See [T1RSLC3](#).

Bit 7: Si Bit of Frame 14 (SiF14).

Bit 6: Si Bit of Frame 12 (SiF12).

Bit 5: Si Bit of Frame 10 (SiF10).

Bit 4: Si Bit of Frame 8 (SiF8).

Bit 3: Si Bit of Frame 6 (SiF6).

Bit 2: Si Bit of Frame 4 (SiF4).

Bit 1: Si Bit of Frame 2 (SiF2).

Bit 0: Si Bit of Frame 0 (SiF0).

Register Name: **E1RSiNAF (E1 Mode Only)**
 Register Description: **Receive Si Bits of the Non-Align Frame Register**
 Register Address: **067h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|------|------|------|------|------|
| Name | SiF15 | SiF13 | SiF11 | SiF9 | SiF7 | SiF5 | SiF3 | SiF1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Si Bit of Frame 15 (SiF15).

Bit 6: Si Bit of Frame 13 (SiF13).

Bit 5: Si Bit of Frame 11 (SiF11).

Bit 4: Si Bit of Frame 9 (SiF9).

Bit 3: Si Bit of Frame 7 (SiF7).

Bit 2: Si Bit of Frame 5 (SiF5).

Bit 1: Si Bit of Frame 3 (SiF3).

Bit 0: Si Bit of Frame 1 (SiF1).

Register Name: **E1RRA (E1 Mode Only)**
 Register Description: **Receive Remote Alarm Register**
 Register Address: **068h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|-------|-------|-------|-------|-------|
| Name | RRAF15 | RRAF13 | RRAF11 | RRAF9 | RRAF7 | RRAF5 | RRAF3 | RRAF1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Remote Alarm Bit of Frame 15 (RRAF15).

Bit 6: Remote Alarm Bit of Frame 13 (RRAF13).

Bit 5: Remote Alarm Bit of Frame 11 (RRAF11).

Bit 4: Remote Alarm Bit of Frame 9 (RRAF9).

Bit 3: Remote Alarm Bit of Frame 7 (RRAF7).

Bit 2: Remote Alarm Bit of Frame 5 (RRAF5).

Bit 1: Remote Alarm Bit of Frame 3 (RRAF3).

Bit 0: Remote Alarm Bit of Frame 1 (RRAF1).

Register Name: **E1RSa4 (E1 Mode Only)**
 Register Description: **Receive Sa4 Bits Register**
 Register Address: **069h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|--------|--------|--------|--------|--------|
| Name | RSa4F15 | RSa4F13 | RSa4F11 | RSa4F9 | RSa4F7 | RSa4F5 | RSa4F3 | RSa4F1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa4 Bit of Frame 15 (RSa4F15).

Bit 6: Sa4 Bit of Frame 13 (RSa4F13).

Bit 5: Sa4 Bit of Frame 11 (RSa4F11).

Bit 4: Sa4 Bit of Frame 9 (RSa4F9).

Bit 3: Sa4 Bit of Frame 7 (RSa4F7).

Bit 2: Sa4 Bit of Frame 5 (RSa4F5).

Bit 1: Sa4 Bit of Frame 3 (RSa4F3).

Bit 0: Sa4 Bit of Frame 1 (RSa4F1).

Register Name: **E1RSa5 (E1 Mode Only)**
 Register Description: **Receive Sa5 Bits Register**
 Register Address: **06Ah + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|--------|--------|--------|--------|--------|
| Name | RSa5F15 | RSa5F13 | RSa5F11 | RSa5F9 | RSa5F7 | RSa5F5 | RSa5F3 | RSa5F1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa5 Bit of Frame 15 (RSa5F15).

Bit 6: Sa5 Bit of Frame 13 (RSa5F13).

Bit 5: Sa5 Bit of Frame 11 (RSa5F11).

Bit 4: Sa5 Bit of Frame 9 (RSa5F9).

Bit 3: Sa5 Bit of Frame 7 (RSa5F7).

Bit 2: Sa5 Bit of Frame 5 (RSa5F5).

Bit 1: Sa5 Bit of Frame 3 (RSa5F3).

Bit 0: Sa5 Bit of Frame 1 (RSa5F1).

Register Name: **E1RSa6 (E1 Mode Only)**
 Register Description: **Receive Sa6 Bits Register**
 Register Address: **06Bh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|--------|--------|--------|--------|--------|
| Name | RSa6F15 | RSa6F13 | RSa6F11 | RSa6F9 | RSa6F7 | RSa6F5 | RSa6F3 | RSa6F1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa6 Bit of Frame 15 (RSa6F15).

Bit 6: Sa6 Bit of Frame 13 (RSa6F13).

Bit 5: Sa6 Bit of Frame 11 (RSa6F11).

Bit 4: Sa6 Bit of Frame 9 (RSa6F9).

Bit 3: Sa6 Bit of Frame 7 (RSa6F7).

Bit 2: Sa6 Bit of Frame 5 (RSa6F5).

Bit 1: Sa6 Bit of Frame 3 (RSa6F3).

Bit 0: Sa6 Bit of Frame 1 (RSa6F1).

Register Name: **E1RSa7 (E1 Mode Only)**
 Register Description: **Receive Sa7 Bits Register**
 Register Address: **06Ch + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|--------|--------|--------|--------|--------|
| Name | RSa7F15 | RSa7F13 | RSa7F11 | RSa7F9 | RSa7F7 | RSa7F5 | RSa7F3 | RSa7F1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa7 Bit of Frame 15 (RSa7F15).

Bit 6: Sa7 Bit of Frame 13 (RSa7F13).

Bit 5: Sa7 Bit of Frame 11 (RSa7F11).

Bit 4: Sa7 Bit of Frame 9 (RSa7F9).

Bit 3: Sa7 Bit of Frame 7 (RSa7F7).

Bit 2: Sa7 Bit of Frame 5 (RSa7F5).

Bit 1: Sa7 Bit of Frame 3 (RSa7F3).

Bit 0: Sa7 Bit of Frame 1 (RSa7F1).

Register Name: **E1RSa8 (E1 Mode Only)**
 Register Description: **Receive Sa8 Bits Register**
 Register Address: **06Dh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|--------|--------|--------|--------|--------|
| Name | RSa8F15 | RSa8F13 | RSa8F11 | RSa8F9 | RSa8F7 | RSa8F5 | RSa8F3 | RSa8F1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa8 Bit of Frame 15 (RSa8F15).

Bit 6: Sa8 Bit of Frame 13 (RSa8F13).

Bit 5: Sa8 Bit of Frame 11 (RSa8F11).

Bit 4: Sa8 Bit of Frame 9 (RSa8F9).

Bit 3: Sa8 Bit of Frame 7 (RSa8F7).

Bit 2: Sa8 Bit of Frame 5 (RSa8F5).

Bit 1: Sa8 Bit of Frame 3 (RSa8F3).

Bit 0: Sa8 Bit of Frame 1 (RSa8F1).

Register Name: **SaBITS**
 Register Description: **Receive SaX Bits Register**
 Register Address: **06Eh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|-----|-----|-----|-----|-----|
| Name | — | — | — | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

This register indicates the last received SaX bit. This can be used in conjunction with the [RLS7](#) register to determine which SaX bits have changed. The user can program which Sa bit positions should be monitored via the [E1RSAIMR](#) register, and when a change is detected through an interrupt in [RLS7.0](#), the user can determine which bit has changed by reading this register and comparing it with previous known values.

Bit 4: Last Received Sa4 Bit (Sa4).

Bit 3: Last Received Sa5 Bit (Sa5).

Bit 2: Last Received Sa6 Bit (Sa6).

Bit 1: Last Received Sa7 Bit (Sa7).

Bit 0: Last Received Sa8 Bit (Sa8).

Register Name: **Sa6CODE**
 Register Description: **Received Sa6 Codeword Register**
 Register Address: **06Fh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|------|------|------|------|
| Name | — | — | — | — | Sa6n | Sa6n | Sa6n | Sa6n |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

This register reports the received Sa6 codeword per ETS 300 233. The bits are monitored on a submultiframe asynchronous basis, so the pattern reported could be one of multiple patterns that would represent a valid codeword. The table below indicates which patterns reported in this register correspond to a given valid Sa6 codeword.

Bits 3 to 0: Sa6 Codeword Bit (Sa6n).

| VALID Sa6 CODE | POSSIBLE REPORTED PATTERNS |
|----------------|----------------------------|
| Sa6_8 | 1000, 0100, 0010, 0001 |
| Sa6_A | 1010, 0101 |
| Sa6_C | 110, 0110, 0011, 1001 |
| Sa6_E | 1110, 0111, 1011, 1101 |
| Sa6_F | 1111 |

Register Name: **RMMR**
 Register Description: **Receive Master Mode Register**
 Register Address: **080h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|-----------|---|---|---|---|--------|-------|
| Name | FRM_EN | INIT_DONE | — | — | — | — | SFTRST | T1/E1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Framer Enable (FRM_EN). This bit must be set to the desired state before writing INIT_DONE.
 0 = Framer disabled—held in low-power state
 1 = Framer enabled—all features active

Bit 6: Initialization Done (INIT_DONE). The user must set this bit once he has written the configuration registers. The host is required to write or clear all device registers prior to setting this bit. Once INIT_DONE is set, the DS26524 will check the FRM_EN bit and, if enabled, will begin operation based on the initial configuration.

Bit 1: Soft Reset (SFTRST). Level sensitive soft reset. Should be taken high then low to reset the receiver.
 0 = Normal operation
 1 = Reset the receiver

Bit 0: Receiver T1/E1 Mode Select (T1/E1). Sets operating mode for receiver only! This bit must be set to the desired state before writing INIT_DONE.
 0 = T1 operation
 1 = E1 operation

Register Name: **RCR1 (T1 Mode)**
 Register Description: **Receive Control Register 1**
 Register Address: **081h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-----|-----|-------|-----|-------|--------|
| Name | SYNCT | RB8ZS | RFM | ARC | SYNCC | RJC | SYNCE | RESYNC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: This register has an alternate definition for E1 mode. See [RCR1](#).

Bit 7: Sync Time (SYNCT).

- 0 = qualify 10 bits
- 1 = qualify 24 bits

Bit 6: Receive B8ZS Enable (RB8ZS).

- 0 = B8ZS disabled
- 1 = B8ZS enabled

Bit 5: Receive Frame Mode Select (RFM).

- 0 = ESF framing mode
- 1 = D4 framing mode

Bit 4: Auto Resync Criteria (ARC).

- 0 = resync on OOF or LOS event
- 1 = resync on OOF only

Bit 3: Sync Criteria (SYNCC).

In D4 Framing Mode:

- 0 = search for Ft pattern, then search for Fs pattern
- 1 = cross couple Ft and Fs pattern

In ESF Framing Mode:

- 0 = search for FPS pattern only
- 1 = search for FPS and verify with CRC-6

Bit 2: Receive Japanese CRC6 Enable (RJC).

- 0 = use ANSI:AT&T:ITU-T CRC-6 calculation (normal operation)
- 1 = use Japanese standard JT-G704 CRC-6 calculation

Bit 1: Sync Enable (SYNCE).

- 0 = auto resync enabled
- 1 = auto resync disabled

Bit 0: Resynchronize (RESYNC). When toggled from low to high, a resynchronization of the receive-side framer is initiated. Must be cleared and set again for a subsequent resync.

Register Name: **RCR1 (E1 Mode)**
 Register Description: **Receive Control Register 1**
 Register Address: **081h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|-------|-------|-------|-------|-----|-------|--------|
| Name | — | RHDB3 | RSIGM | RG802 | RCRC4 | FRC | SYNCE | RESYNC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: This register has an alternate definition for T1 mode. See [RCR1](#).

Bit 6: Receive HDB3 Enable (RHDB3).

0 = HDB3 disabled

1 = HDB3 enabled (decoded per O.162)

Bit 5: Receive-Signaling Mode Select (RSIGM).

0 = CAS signaling mode

1 = CCS signaling mode

Bit 4: Receive G.802 Enable (RG802). See [Figure 10-23](#) for details.

0 = do not force RCHBLK high during bit 1 of time slot 26

1 = force RCHBLK high during bit 1 of time slot 26

Bit 3: Receive CRC-4 Enable (RCRC4).

0 = CRC-4 disabled

1 = CRC-4 enabled

Bit 2: Frame Resync Criteria (FRC).

0 = resync if FAS received in error three consecutive times

1 = resync if FAS or bit 2 of non-FAS is received in error three consecutive times

Bit 1: Sync Enable (SYNCE).

0 = auto resync enabled

1 = auto resync disabled

Bit 0: Resynchronize (RESYNC). When toggled from low to high, a resynchronization of the receive-side framer is initiated. Must be cleared and set again for a subsequent resync.

Register Name: **T1RIBCC (T1 Mode)**
 Register Description: **Receive In-Band Code Control Register**
 Register Address: **082h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| | | | | | | | | |
|---------|---|---|------|------|------|------|------|------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | — | RUP2 | RUP1 | RUP0 | RDN2 | RDN1 | RDN0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: This register has an alternate definition for E1 mode. See [E1RCR2](#).

Bits 5 to 3: Receive Up Code Length Definition Bits (RUP[2:0]).

| RUP2 | RUP1 | RUP0 | LENGTH SELECTED |
|------|------|------|-----------------|
| 0 | 0 | 0 | 1 bits |
| 0 | 0 | 1 | 2 bits |
| 0 | 1 | 0 | 3 bits |
| 0 | 1 | 1 | 4 bits |
| 1 | 0 | 0 | 5 bits |
| 1 | 0 | 1 | 6 bits |
| 1 | 1 | 0 | 7 bits |
| 1 | 1 | 1 | 8 : 16 bits |

Bits 2 to 0: Receive Down Code Length Definition Bits (RDN[2:0]).

| RDN2 | RDN1 | RDN0 | LENGTH SELECTED |
|------|------|------|-----------------|
| 0 | 0 | 0 | 1 bits |
| 0 | 0 | 1 | 2 bits |
| 0 | 1 | 0 | 3 bits |
| 0 | 1 | 1 | 4 bits |
| 1 | 0 | 0 | 5 bits |
| 1 | 0 | 1 | 6 bits |
| 1 | 1 | 0 | 7 bits |
| 1 | 1 | 1 | 8 : 16 bits |

Register Name: **E1RCR2 (E1 Mode)**
 Register Description: **Receive Control Register 2**
 Register Address: **082h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|---|---|-------|
| Name | RSa8S | RSa7S | RSa6S | RSa5S | RSa4S | — | — | RLOSA |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: This register has an alternate definition for T1 mode. See [T1RIBCC](#).

Bit 7: Sa8 Bit Select (RSa8S). Set to one to have RLCLK pulse at the Sa8 bit position; set to zero to force RLCLK low during Sa8 bit position.

Bit 6: Sa7 Bit Select (RSa7S). Set to one to have RLCLK pulse at the Sa7 bit position; set to zero to force RLCLK low during Sa7 bit position.

Bit 5: Sa6 Bit Select (RSa6S). Set to one to have RLCLK pulse at the Sa6 bit position; set to zero to force RLCLK low during Sa6 bit position.

Bit 4: Sa5 Bit Select (RSa5S). Set to one to have RLCLK pulse at the Sa5 bit position; set to zero to force RLCLK low during Sa5 bit position.

Bit 3: Sa4 Bit Select (RSa4S). Set to one to have RLCLK pulse at the Sa4 bit position; set to zero to force RLCLK low during Sa4 bit position.

Bit 0: Receive Loss of Signal Alternate Criteria (RLOSA). Defines the criteria for a loss-of-signal condition.

0 = LOS declared upon 255 consecutive zeros (125µs)

1 = LOS declared upon 2048 consecutive zeros (1ms)

Register Name: **RCR3**
 Register Description: **Receive Control Register 3**
 Register Address: **083h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|---|-------|---|---|---|-----|-----|
| Name | IDF | — | RSERC | — | — | — | PLB | FLB |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Input Data Format (IDF).

0 = bipolar data is expected at RTIP and RRING (either AMI or B8ZS)

1 = NRZ data is expected at RTIP. The BPV counter will be disabled and RRING will be ignored by the DS26524.

Bit 5: RSER Control (RSERC).

0 = allow RSER to output data as received under all conditions (normal operation)

1 = force RSER to one under loss of frame alignment conditions

Bit 1: Payload Loopback (PLB).

0 = loopback disabled

1 = loopback enabled

When PLB is enabled, the following will occur:

- 1) Data will be transmitted from the TTIP and TRING pins synchronous with RCLK instead of TCLK.
- 2) All the receive-side signals will continue to operate normally.
- 3) The TCHCLK and TCHBLK signals are forced low.
- 4) Data at the TSER, TDATA, and TSIG pins is ignored.
- 5) The TLCLK signal will become synchronous with RCLK instead of TCLK.

In a PLB situation, the DS26524 loops the 192 bits (248 for E1) of payload data (with BPVs corrected) from the receive section back to the transmit section. The transmitter follows the frame alignment provided by the receiver. The receive frame boundary is automatically fed into the transmit section, such that the transmit frame position is locked to the receiver (i.e., TSYNC is sourced from RSYNC). The FPS framing pattern, CRC-6 calculation, and the FDL bits (FAS word, Si, Sa, E-bits, and CRC-4 for E1) are not looped back. Rather, they are reinserted by the DS26524 (i.e., the transmit section will modify the payload as if it was input at TSER).

Bit 0: Framer Loopback (FLB).

0 = loopback disabled

1 = loopback enabled

This loopback is useful in testing and debugging applications. In FLB, the DS26524 loops data from the transmit side back to the receive side. When FLB is enabled, the following will occur:

- 1) (T1 mode) An unframed all-ones code will be transmitted at TTIP and TRING.
(E1 mode) Normal data will be transmitted at TTIP and TRING.
- 2) Data at RTIP and RRING will be ignored.
- 3) All receive-side signals will take on timing synchronous with TCLK instead of RCLK.
- 4) Note that it is not acceptable to have RCLK tied to TCLK during this loopback because this will cause an unstable condition.

Register Name: **RIOCR**
 Register Description: **Receive I/O Configuration Register**
 Register Address: **084h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------------|-----------------|---------------|---------------|------|-------------|--------------|--------------|
| Name | RCLKINV | RSYNCINV | H100EN | RSCLKM | RSMS | RSIO | RSMS2 | RSMS1 |
| | <i>RCLKINV</i> | <i>RSYNCINV</i> | <i>H100EN</i> | <i>RSCLKM</i> | — | <i>RSIO</i> | <i>RSMS2</i> | <i>RSMS1</i> |
| Default | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

Bit 7: RCLK Invert (RCLKINV).

0 = no inversion
 1 = invert RCLK as input

Bit 6: RSYNC Invert (RSYNCINV).

0 = no inversion
 1 = invert RSYNC as either input or output

Bit 5: H.100 SYNC Mode (H100EN). See Section [8.8.3](#) for more information.

0 = normal operation
 1 = RSYNC and TSSYNCIO signals are shifted

Bit 4: RSYCLK Mode Select (RSCLKM).

0 = if RSYCLK is 1.544MHz
 1 = if RSYCLK is 2.048MHz or IBO enabled

Bit 3: RSYNC Multiframe Skip Control (RSMS) (T1 Mode Only). Useful in framing format conversions from D4 to ESF. This function is not available when the receive-side elastic store is enabled. RSYNC must be set to output multiframe pulses.

0 = RSYNC will output a pulse at every multiframe
 1 = RSYNC will output a pulse at every other multiframe

Bit 2: RSYNC I/O Select (RSIO). (**Note:** This bit must be set to zero when elastic store is disabled) The default value for this bit is a logic 1 so that the default state of RSYNC is as an input.

0 = RSYNC is an output
 1 = RSYNC is an input (only valid if elastic store enabled)

Bit 1: RSYNC Mode Select 2 (RSMS2).

T1 Mode: RSYNC pin must be programmed in the output frame mode.

0 = do not pulse double-wide in signaling frames
 1 = do pulse double-wide in signaling frames

E1 Mode: RSYNC pin must be programmed in the output multiframe mode.

0 = RSYNC outputs CAS multiframe boundaries
 1 = RSYNC outputs CRC-4 multiframe boundaries

In E1 mode, RSMS2 also selects which multiframe signal is available at the RMSYNC pin, regardless of the configuration for RSYNC. When RSMS2 = 0, RMSYNC outputs CAS multiframe boundaries; when RSMS2 = 1, RMSYNC outputs CRC-4 multiframe boundaries.

Bit 0: RSYNC Mode Select 1 (RSMS1). Selects frame or multiframe pulse when RSYNC pin is in output mode. In input mode (elastic store must be enabled) multiframe mode is only useful when receive-signaling reinsertion is enabled.

0 = frame mode
 1 = multiframe mode

Register Name: **RESCR**
 Register Description: **Receive Elastic Store Control Register**
 Register Address: **085h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---|------|---------|------|--------|------|
| Name | RDATFMT | RGCLKEN | — | RSZS | RESALGN | RESR | RESMDM | RESE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive Channel Data Format (RDATFMT).

- 0 = 64kbps (data contained in all 8 bits)
- 1 = 56kbps (data contained in 7 out of the 8 bits)

Bit 6: Receive Gapped Clock Enable (RGCLKEN).

- 0 = RCHCLK functions normally
- 1 = Enable gapped bit clock output on RCHCLK

Note: *RGPKEN and RDATFMT are not associated with the elastic store and are explained in the fractional support section.*

Bit 4: Receive Slip Zone Select (RSZS). This bit determines the minimum distance allowed between the elastic store read and write pointers before forcing a controlled slip. This bit only applies during T1-to-E1 or E1-to-T1 conversion applications.

- 0 = force a slip at 9 bytes or less of separation (used for clustered blank channels)
- 1 = force a slip at 2 bytes or less of separation (used for distributed blank channels and minimum delay mode)

Bit 3: Receive Elastic Store Align (RESALGN). Setting this bit from 0 to 1 forces the receive elastic store's write/read pointers to a minimum separation of half a frame. No action is taken if the pointer separation is already greater or equal to half a frame. If pointer separation is less than half a frame, the command is executed and the data is disrupted. Should be toggled after RSYCLK has been applied and is stable. Must be cleared and set again for a subsequent align.

Bit 2: Receive Elastic Store Reset (RESR). Setting this bit from 0 to 1 forces the read pointer into the same frame that the write pointer is exiting, minimizing the delay through the elastic store. If this command should place the pointers within the slip zone (see bit 4), then an immediate slip occurs and the pointers move back to opposite frames. Should be toggled after RSYCLK has been applied and is stable. Do not leave this bit set HIGH.

Bit 1: Receive Elastic Store Minimum Delay Mode (RESMDM).

- 0 = elastic stores operate at full two-frame depth
- 1 = elastic stores operate at 32-bit depth

Bit 0: Receive Elastic Store Enable (RESE).

- 0 = elastic store is bypassed
- 1 = elastic store is enabled

Register Name: **ERCNT**
 Register Description: **Error-Counter Configuration Register**
 Register Address: **086h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------------|-------------|-------------|-------------|-------------|------|--------|---------------|
| Name | 1SECS | MCUS | MECU | ECUS | EAMS | FSBE | MOSCRF | LCVCRF |
| | <i>1SECS</i> | <i>MCUS</i> | <i>MECU</i> | <i>ECUS</i> | <i>EAMS</i> | — | — | <i>LCVCRF</i> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: One-Second Select (1SECS). This bit allows for synchronization of the error counter updates between multiple ports. When ERCNT.3 = 0, setting this bit (on a specific framer) will update the framer's error counters on the transition of the one-second timer from framer 1. Note that this bit should always be clear for framer 1.

- 0 = use the one-second timer that is internal to the framer
- 1 = use the one-second timer from framer 1 to latch updates

Bit 6: Manual Counter Update Select (MCUS). When manual update mode is enabled with EAMS, this bit can be used to allow the incoming LATCH_CNT signal to latch all counters.

- 0 = MECU is used to manually latch counters
- 1 = counters are latched on the rising edge of the LATCH_CNT signal

Bit 5: Manual Error Counter Update (MECU). When enabled by ERCNT.3, the changing of this bit from 0 to 1 allows the next clock cycle to load the error counter registers with the latest counts and reset the counters. The user must wait a minimum of 250µs before reading the error count registers to allow for proper update.

Bit 4: Error Counter Update Select (ECUS).

T1 Mode:

- 0 = update error counters once a second
- 1 = update error counters every 42ms (333 frames)

E1 Mode:

- 0 = update error counters once a second
- 1 = update error counters every 62.5ms (500 frames)

Bit 3: Error Accumulation Mode Select (EAMS).

- 0 = automatic updating of error counters enabled. The state of ERCNT.4 determines accumulation time (timed update)
- 1 = user toggling of ERCNT.5 determines accumulation time (manual update)

Bit 2: PCVCR Fs-Bit Error Report Enable (FSBE) (T1 Mode Only).

- 0 = do not report bit errors in Fs-bit position; only Ft-bit position
- 1 = report bit errors in Fs-bit position as well as Ft-bit position

Bit 1: Multiframe Out of Sync Count Register Function Select (MOSCRF) (T1 Mode Only).

- 0 = count errors in the framing bit position
- 1 = count the number of multiframe out of sync

Bit 0: T1 Line Code Violation Count Register Function Select (LCVCRF).

- 0 = do not count excessive zeros
- 1 = count excessive zeros

Register Name: **RHFC**
 Register Description: **Receive HDLC FIFO Control Register**
 Register Address: **087h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| | | | | | | | | |
|---------|---|---|---|---|---|---|--------|--------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | — | — | — | — | — | RFHWM1 | RFHWM0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 1 and 0: Receive FIFO High Watermark Select (RFHWM[1:0]).

| RFHWM1 | RFHWM0 | RECEIVE FIFO WATERMARK (BYTES) |
|--------|--------|--------------------------------|
| 0 | 0 | 4 |
| 0 | 1 | 16 |
| 1 | 0 | 32 |
| 1 | 1 | 48 |

Register Name: **RIBOC**
 Register Description: **Receive Interleave Bus Operation Control Register**
 Register Address: **088h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| | | | | | | | | |
|---------|---|------|------|--------|-------|-----|-----|-----|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | IBS1 | IBS0 | IBOSEL | IBOEN | DA2 | DA1 | DA0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 6 and 5: IBO Bus Size Bits (IBS[1:0]). Indicates how many devices on the bus.

| IBS1 | IBS0 | BUS SIZE |
|------|------|------------------------------|
| 0 | 0 | 2 devices on bus (4.096MHz) |
| 0 | 1 | 4 devices on bus (8.192MHz) |
| 1 | 0 | 8 devices on bus (16.384MHz) |
| 1 | 1 | Reserved for future use |

Bit 4: Interleave Bus Operation Select (IBOSEL). This bit selects channel or frame interleave mode.
 0 = Channel Interleave
 1 = Frame Interleave

Bit 3: Interleave Bus Operation Enable (IBOEN).
 0 = interleave bus operation disabled
 1 = interleave bus operation enabled

Bits 2 to 0: Device Assignment Bits (DA[2:0]).

| DA2 | DA1 | DA0 | DEVICE POSITION |
|-----|-----|-----|-------------------|
| 0 | 0 | 0 | 1st device on bus |
| 0 | 0 | 1 | 2nd device on bus |
| 0 | 1 | 0 | 3rd device on bus |
| 0 | 1 | 1 | 4th device on bus |
| 1 | 0 | 0 | 5th device on bus |
| 1 | 0 | 1 | 6th device on bus |
| 1 | 1 | 0 | 7th device on bus |
| 1 | 1 | 1 | 8th device on bus |

Register Name: **T1RSCC (T1 Mode Only)**
 Register Description: **In-Band Receive Spare Control Register**
 Register Address: **089h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| | | | | | | | | |
|---------|---|---|---|---|---|------|------|------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | — | — | — | — | RSC2 | RSC1 | RSC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 2 to 0: Receive Spare Code Length Definition Bits (RSC[2:0]).

| RSC2 | RSC1 | RSC0 | LENGTH SELECTED (BITS) |
|------|------|------|------------------------|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 3 |
| 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 5 |
| 1 | 0 | 1 | 6 |
| 1 | 1 | 0 | 7 |
| 1 | 1 | 1 | 8:16 |

Register Name: **RXPC**
 Register Description: **Receive Expansion Port Control Register**
 Register Address: **08Ah + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| | | | | | | | | |
|---------|---|---|---|---|---|--------|--------|-------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | — | — | — | — | RBPDIR | RBPFUS | RBPEN |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 2: Receive BERT Port Direction Control (RBPDIR).

0 = Normal (line) operation. Receive BERT port receives data from the receive framer.

1 = System (backplane) operation. Receive BERT port receives data from the transmit path. The transmit path enters the receive BERT on the line side of the elastic store (if enabled).

Bit 1: Receive BERT Port Framed/Unframed Select (RBPFUS) (T1 Mode Only).

0 = The receive BERT will *not* clock data from the F-bit position (framed).

1 = The receive BERT will clock data from the F-bit position (unframed).

Bit 0: Receive BERT Port Enable (RBPEN).

0 = Receive BERT port is not active.

1 = Receive BERT port is active.

Register Name: **RBPBS**
 Register Description: **Receive BERT Port Bit Suppress Register**
 Register Address: **08Bh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Name | BPBSE8 | BPBSE7 | BPBSE6 | BPBSE5 | BPBSE4 | BPBSE3 | BPBSE2 | BPBSE1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive Channel Bit 8 Suppress (BPBSE8). MSB of the channel. Set to one to stop this bit from being used.

Bit 6: Receive Channel Bit 7 Suppress (BPBSE7). Set to one to stop this bit from being used.

Bit 5: Receive Channel Bit 6 Suppress (BPBSE6). Set to one to stop this bit from being used.

Bit 4: Receive Channel Bit 5 Suppress (BPBSE5). Set to one to stop this bit from being used.

Bit 3: Receive Channel Bit 4 Suppress (BPBSE4). Set to one to stop this bit from being used.

Bit 2: Receive Channel Bit 3 Suppress (BPBSE3). Set to one to stop this bit from being used.

Bit 1: Receive Channel Bit 2 Suppress (BPBSE2). Set to one to stop this bit from being used.

Bit 0: Receive Channel Bit 1 Suppress (BPBSE1). LSB of the channel. Set to one to stop this bit from being used.

Register Name: **RLS1**
 Register Description: **Receive Latched Status Register 1**
 Register Address: **090h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | RRAIC | RAISC | RLOSC | RLOFC | RRAID | RAISD | RLOSD | RLOFD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are latched and can create interrupts.

Bit 7: Receive Remote Alarm Indication Condition Clear (RRAIC). Falling edge detect of RRAI. Set when a RRAI condition has cleared.

Bit 6: Receive Alarm Indication Signal Condition Clear (RAISC). Falling edge detect of RAIS. Set when a RAIS condition has cleared.

Bit 5: Receive Loss of Signal Condition Clear (RLOSC). Falling edge detect of RLOS. Set when an RLOS condition has cleared.

Bit 4: Receive Loss of Frame Condition Clear (RLOFC). Falling edge detect of RLOF. Set when an RLOF condition has cleared.

Bit 3: Receive Remote Alarm Indication Condition Detect (RRAID). Rising edge detect of RRAI. Set when a remote alarm is received at RTIP and RRING.

Bit 2: Receive Alarm Indication Signal Condition Detect (RAISD). Rising edge detect of RAIS. Set when an unframed all-ones code is received at RTIP and RRING.

Bit 1: Receive Loss of Signal Condition Detect (RLOSD). Rising edge detect of RLOS. Set when 192 consecutive zeros have been detected at RTIP and RRING.

Bit 0: Receive Loss of Frame Condition Detect (RLOFD). Rising edge detect of RLOF. Set when the DS26524 has lost synchronized to the received data stream.

Register Name: **RLS2 (T1 Mode)**
 Register Description: **Receive Latched Status Register 2**
 Register Address: **091h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|---|------|-----|------|------|------|-----|
| Name | RPDV | — | COFA | 8ZD | 16ZD | SEFE | B8ZS | FBE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in these register are latched. This register does not create interrupts. See [RLS2](#) for E1 mode.

Bit 7: Receive Pulse Density Violation Event (RPDV). Set when the receive data stream does not meet the ANSI T1.403 requirements for pulse density.

Bit 5: Change of Frame Alignment Event (COFA). Set when the last resync resulted in a change of frame or multiframe alignment.

Bit 4: Eight Zero Detect Event (8ZD). Set when a string of at least eight consecutive zeros (regardless of the length of the string) have been received.

Bit 3: Sixteen Zero Detect Event (16ZD). Set when a string of at least 16 consecutive zeros (regardless of the length of the string) have been received.

Bit 2: Severely Errored Framing Event (SEFE). Set when two out of six framing bits (Ft or FPS) are received in error.

Bit 1: B8ZS Codeword Detect Event (B8ZS). Set when a B8ZS codeword is detected at RTIP and RRING independent of whether the B8ZS mode is selected or not. Useful for automatically setting the line coding.

Bit 0: Frame Bit Error Event (FBE). Set when a Ft (D4) or FPS (ESF) framing bit is received in error.

Register Name: **RLS2 (E1 Mode)**
 Register Description: **Receive Latched Status Register 2**
 Register Address: **091h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|-------|-------|-------|------|------|------|-----|
| Name | — | CRCRC | CASRC | FASRC | RSA1 | RSA0 | RCMF | RAF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are latched. Bits 0 to 3 can cause interrupts. There is no associated real-time register. See [RLS2](#) for T1 mode.

Bit 6: CRC Resync Criteria Met Event (CRCRC). Set when 915:1000 codewords are received in error.

Bit 5: CAS Resync Criteria Met Event (CASRC). Set when two consecutive CAS MF alignment words are received in error.

Bit 4: FAS Resync Criteria Met Event (FASRC). Set when three consecutive FAS words are received in error.

Bit 3: Receive-Signaling All-Ones Event (RSA1). Set when the contents of time slot 16 contains fewer than three zeros over 16 consecutive frames. This alarm is not disabled in the CCS signaling mode.

Bit 2: Receive-Signaling All-Zeros Event (RSA0). Set when over a full MF, time slot 16 contains all zeros.

Bit 1: Receive CRC-4 Multiframe Event (RCMF). Set on CRC-4 multiframe boundaries. This bit continues to be set every 2ms on an arbitrary boundary if CRC-4 is disabled.

Bit 0: Receive Align Frame Event (RAF). Set approximately every 250 μ s to alert the host that Si and Sa bits are available in the RAF and RNAF registers.

Register Name: **RLS3 (T1 Mode)**
 Register Description: **Receive Latched Status Register 3**
 Register Address: **092h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|------|------|------|-------|------|------|------|
| Name | LORCC | LSPC | LDNC | LUPC | LORCD | LSPD | LDND | LUPD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are latched and can create interrupts. See [RLS3](#) for E1 mode.

Bit 7: Loss of Receive Clock Condition Clear (LORCC). Falling edge detect of LORC. Set when an LORC condition was detected and then removed.

Bit 6: Spare Code Detected Condition Clear (LSPC). Falling edge detect of LSP. Set when a spare-code match condition was detected and then removed.

Bit 5: Loop-Down Code Detected Condition Clear (LDNC). Falling edge detect of LDN. Set when a loop-down condition was detected and then removed.

Bit 4: Loop-Up Code Detected Condition Clear (LUPC). Falling edge detect of LUP. Set when a loop-up condition was detected and then removed.

Bit 3: Loss of Receive Clock Condition Detect (LORCD). Rising edge detect of LORC. Set when the RCLK pin has not transitioned for one channel time.

Bit 2: Spare Code Detected Condition Detect (LSPD). Rising edge detect of LSP. Set when the spare code as defined in the [T1RSCD1:T1RSCD2](#) registers is being received.

Bit 1: Loop-Down Code Detected Condition Detect (LDND). Rising edge detect of LDN. Set when the loop-down code as defined in the [T1RDNCD1:T1RDNCD2](#) register is being received.

Bit 0: Loop-Up Code Detected Condition Detect (LUPD). Rising edge detect of LUP. Set when the loop-up code as defined in the [T1RUPCD1:T1RUPCD2](#) register is being received.

Register Name: **RLS3 (E1 Mode)**
 Register Description: **Receive Latched Status Register 3**
 Register Address: **092h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|---|---------|-------|-------|---|---------|-------|
| Name | LORCC | — | V52LNKC | RDMAC | LORCD | — | V52LNKD | RDMAD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are latched and can create interrupts. See [RLS3](#) for T1 mode.

Bit 7: Loss of Receive Clock Clear (LORCC). Change of state indication. Set when an LORC condition has cleared (falling edge detect of LORC)

Bit 5: V5.2 Link Detected Clear (V52LNKC). Change of state indication. Set when a V52LNK condition has cleared (falling edge detect of V52LNK).

Bit 4: Receive Distant MF Alarm Clear (RDMAC). Change of state indication. Set when an RDMA condition has cleared (falling edge detect of RDMA).

Bit 3: Loss of Receive Clock Detect (LORCD). Change of state indication. Set when the RCLK pin has not transitioned for one channel time (rising edge detect of LORC).

Bit 1: V5.2 Link Detect (V52LNKD). Change of state indication. Set on detection of a V5.2 link identification signal. (G.965). This is the rising edge detect of V52LNK.

Bit 0: Receive Distant MF Alarm Detect (RDMAD). Change of state indication. Set when bit 6 of time slot 16 in frame 0 has been set for two consecutive multiframes. This alarm is not disabled in the CCS signaling mode. This is the rising edge detect of RDMA.

Register Name: **RLS4**
 Register Description: **Receive Latched Status Register 4**
 Register Address: **093h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|-------|-------|---|-------|------|-------|-----|
| Name | RESF | RESEM | RSLIP | — | RSCOS | 1SEC | TIMER | RMF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are latched and can create interrupts.

Bit 7: Receive Elastic Store Full Event (RESF). Set when the receive elastic store buffer fills and a frame is deleted.

Bit 6: Receive Elastic Store Empty Event (RESEM). Set when the receive elastic store buffer empties and a frame is repeated.

Bit 5: Receive Elastic Store Slip Occurrence Event (RSLIP). Set when the receive elastic store has either repeated or deleted a frame.

Bit 3: Receive-Signaling Change-of-State Event (RSCOS). Set when any channel selected by the Receive-Signaling Change-of-State Interrupt Enable registers ([RSCSE1](#):RSCSE3) changes signaling state.

Bit 2: One-Second Timer (1SEC). Set on every one-second interval based on RCLK.

Bit 1: Timer Event (TIMER). This status bit indicates that the performance monitor counters have been updated and are available to be read by the host. The error counter update interval as determined by the settings in the Error Counter Configuration register ([ERCNT](#)).

T1 Mode: Set on increments of one second or 42ms based on RCLK, or a manual latch event.

E1 Mode: Set on increments of one second or 62.5ms based on RCLK, or a manual latch event.

Bit 0: Receive Multiframe Event (RMF).

T1 Mode: Set every 1.5ms on D4 MF boundaries or every 3ms on ESF MF boundaries.

E1 Mode: Set every 2.0ms on receive CAS multiframe boundaries to alert host the signaling data is available. Continues to set on an arbitrary 2.0ms boundary when CAS signaling is not enabled.

Register Name: **RLS5**
 Register Description: **Receive Latched Status Register 5 (HDLC)**
 Register Address: **094h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|------|-------|-----|-----|-------|------|
| Name | — | — | ROVR | RHOBT | RPE | RPS | RHWMS | RNES |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are latched and can cause interrupts.

Bit 5: Receive FIFO Overrun (ROVR). Set when the receive HDLC controller has terminated packet reception because the FIFO buffer is full.

Bit 4: Receive HDLC Opening Byte Event (RHOBT). Set when the next byte available in the receive FIFO is the first byte of a message.

Bit 3: Receive Packet-End Event (RPE). Set when the HDLC controller detects either the finish of a valid message (i.e., CRC check complete) or when the controller has experienced a message fault such as a CRC checking error, or an overrun condition, or an abort has been seen. This is a latched bit and will be cleared when read.

Bit 2: Receive Packet-Start Event (RPS). Set when the HDLC controller detects an opening byte. This is a latched bit and will be cleared when read.

Bit 1: Receive FIFO Above High Watermark Set Event (RHWMS). Set when the receive 64-byte FIFO crosses the high watermark as defined by the Receive HDLC FIFO Control register ([RHFC](#)). Rising edge detect of RHWM.

Bit 0: Receive FIFO Not Empty Set Event (RNES). Set when the receive FIFO has transitioned from empty to not empty (at least one byte has been put into the FIFO). Rising edge detect of RNE.

Register Name: **RLS7 (T1 Mode)**
 Register Description: **Receive Latched Status Register 7**
 Register Address: **096h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---------|---------|--------|-------|----|----|
| Name | — | — | RRAI-CI | RAIS-CI | RSLC96 | RFDLF | BC | BD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are latched and can create interrupts. See [RLS7](#) for E1 mode.

Bit 5: Receive RAI-CI Detect (RRAI-CI). Set when an RAI-CI pattern has been detected by the receiver. This bit is active in ESF framing mode only, and will set only if an RAI condition is being detected ([RRTS1.3](#)). When the host reads (and clears) this bit, it will set again each time the RAI-CI pattern is detected (approximately every 1.1 seconds).

Bit 4: Receive AIS-CI Detect (RAIS-CI). Set when an AIS-CI pattern has been detected by the receiver. This bit will set only if an AIS condition is being detected ([RRTS1.2](#)). This is a latched bit that must be cleared by the host, and will set again each time the AIS-CI pattern is detected (approximately every 1.2 seconds).

Bit 3: Receive SLC-96 Alignment Event (RSLC96). Set when a valid SLC-96 alignment pattern is detected in the Fs-bit stream, and the RSLCx registers have data available for retrieval. See Section [8.9.4.5](#) for more information.

Bit 2: Receive FDL Register Full Event (RFDLF). Set when the 8-bit [T1RFDL](#) register is full. Useful for SLC-96 operation, or manual extraction of FDL data bits. See Section [8.9.5.4](#) for more information.

Bit 1: BOC Clear Event (BC). Set when a valid BOC is no longer detected (with the disintegration filter applied).

Bit 0: BOC Detect Event (BD). Set when a valid BOC has been detected (with the BOC filter applied).

Register Name: **RLS7 (E1 Mode)**
 Register Description: **Receive Latched Status Register 7**
 Register Address: **096h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|-------|-------|
| Name | — | — | — | — | — | — | Sa6CD | SaXCD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are latched and can create interrupts. See [RLS7](#) for T1 mode.

Bit 1: Sa6 Codeword Detect (Sa6CD). Set when a valid codeword (per ETS 300 233) is detected in the Sa6 bit positions.

Bit 0: SaX Bit Change Detect (SaXCD). Set when a bit change is detected in the SaX bit position. The enabled SaX bits are selected by the [E1RSAIMR](#) register.

Register Name: **RSS1, RSS2, RSS3, RSS4**
 Register Description: **Receive-Signaling Status Registers 1 to 4**
 Register Address: **098h, 099h, 09Ah, 09Bh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | (MSB) 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) | |
|---------|---------|------|------|------|------|------|------|---------|--------------------------------------|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1* | RSS1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | RSS2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17* | RSS3 |
| | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | RSS4 (E1 Mode Only) |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Note: Status bits in this register are latched.

When a channel's signaling data changes state, the respective bit in registers [RSS1:RSS4](#) will be set and latched. The RSCOS bit ([RLS4.3](#)) will be set if the channel was also enabled by setting the appropriate bit in [RSCSE1:4](#). The $\overline{\text{INTB}}$ signal will go low if enabled by the interrupt mask bit [RIM4.3](#). The bit will remain set until read.

*Note that in E1 CAS mode, the LSB of RSS1 would typically represent the CAS alignment bits, and the LSB of [RSS3](#) represents reserved bits and the distant multiframe alarm.

Register Name: **T1RSCD1 (T1 Mode Only)**
 Register Description: **Receive Spare Code Definition Register 1**
 Register Address: **09Ch + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: Writing this register resets the detector's integration period.

Bit 7: Receive Spare Code Definition Bit 7 (C7). First bit of the repeating pattern.

Bit 6: Receive Spare Code Definition Bit 6 (C6). A Don't Care if a 1-bit length is selected.

Bit 5: Receive Spare Code Definition Bit 5 (C5). A Don't Care if a 1- or 2-bit length is selected.

Bit 4: Receive Spare Code Definition Bit 4 (C4). A Don't Care if a 1- to 3-bit length is selected.

Bit 3: Receive Spare Code Definition Bit 3 (C3). A Don't Care if a 1- to 4-bit length is selected.

Bit 2: Receive Spare Code Definition Bit 2 (C2). A Don't Care if a 1- to 5-bit length is selected.

Bit 1: Receive Spare Code Definition Bit 1 (C1). A Don't Care if a 1- to 6-bit length is selected.

Bit 0: Receive Spare Code Definition Bit 0 (C0). A Don't Care if a 1- to 7-bit length is selected.

Register Name: **T1RSCD2 (T1 Mode Only)**
 Register Description: **Receive Spare Code Definition Register 2**
 Register Address: **09Dh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive Spare Code Definition Bit 7 (C7). A Don't Care if a 1- to 7-bit length is selected.

Bit 6: Receive Spare Code Definition Bit 6 (C6). A Don't Care if a 1- to 7-bit length is selected.

Bit 5: Receive Spare Code Definition Bit 5 (C5). A Don't Care if a 1- to 7-bit length is selected.

Bit 4: Receive Spare Code Definition Bit 4 (C4). A Don't Care if a 1- to 7-bit length is selected.

Bit 3: Receive Spare Code Definition Bit 3 (C3). A Don't Care if a 1- to 7-bit length is selected.

Bit 2: Receive Spare Code Definition Bit 2 (C2). A Don't Care if a 1- to 7-bit length is selected.

Bit 1: Receive Spare Code Definition Bit 1 (C1). A Don't Care if a 1- to 7-bit length is selected.

Bit 0: Receive Spare Code Definition Bit 0 (C0). A Don't Care if a 1- to 7-bit length is selected.

Register Name: **RIIR**
 Register Description: **Receive Interrupt Information Register**
 Register Address: **09Fh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|------|-------|------|------|------|--------|------|
| Name | — | RLS7 | RLS6* | RLS5 | RLS4 | RLS3 | RLS2** | RLS1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

*RLS6 is reserved for future use.

**Currently, RLS2 does not create an interrupt, therefore this bit is not used in T1 mode.

The Receive Interrupt Information register ([RIIR](#)) indicates which of the DS26524 status registers are generating an interrupt. When an interrupt occurs, the host can read RIIR to quickly identify which of the receive status registers is (are) causing the interrupt(s). The RIIR bits clear once the appropriate interrupt has been serviced and cleared, as long as no additional, unmasked interrupt condition is present in the associated status register. Status bits that have been masked via the Receive Interrupt Mask (RIMx) registers will also be masked from the RIIR register.

Register Name: **RIM1**
 Register Description: **Receive Interrupt Mask Register 1**
 Register Address: **0A0h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | RRAIC | RAISC | RLOSC | RLOFC | RRAID | RAISD | RLOSD | RLOFD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive Remote Alarm Indication Condition Clear (RRAIC).

0 = interrupt masked
 1 = interrupt enabled

Bit 6: Receive Alarm Indication Signal Condition Clear (RAISC).

0 = interrupt masked
 1 = interrupt enabled

Bit 5: Receive Loss of Signal Condition Clear (RLOSC).

0 = interrupt masked
 1 = interrupt enabled

Bit 4: Receive Loss of Frame Condition Clear (RLOFC).

0 = interrupt masked
 1 = interrupt enabled

Bit 3: Receive Remote Alarm Indication Condition Detect (RRAID).

0 = interrupt masked
 1 = interrupt enabled

Bit 2: Receive Alarm Indication Signal Condition Detect (RAISD).

0 = interrupt masked
 1 = interrupt enabled

Bit 1: Receive Loss of Signal Condition Detect (RLOSD).

0 = interrupt masked
 1 = interrupt enabled

Bit 0: Receive Loss of Frame Condition Detect (RLOFD).

0 = interrupt masked
 1 = interrupt enabled

Register Name: **RIM2 (E1 Mode Only)**
 Register Description: **Receive Interrupt Mask Register 2**
 Register Address: **0A1h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|------|------|------|-----|
| Name | — | — | — | — | RSA1 | RSA0 | RCMF | RAF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 3: Receive-Signaling All-Ones Event (RSA1).

0 = interrupt masked
 1 = interrupt enabled

Bit 2: Receive-Signaling All-Zeros Event (RSA0).

0 = interrupt masked
 1 = interrupt enabled

Bit 1: Receive CRC-4 Multiframe Event (RCMF).

0 = interrupt masked
 1 = interrupt enabled

Bit 0: Receive Align Frame Event (RAF).

0 = interrupt masked
 1 = interrupt enabled

Register Name: **RIM3 (T1 Mode)**
 Register Description: **Receive Interrupt Mask Register 3**
 Register Address: **0A2h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|------|------|------|-------|------|------|------|
| Name | LORCC | LSPC | LDNC | LUPC | LORCD | LSPD | LDND | LUPD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: For E1 mode, see [RIM3](#).

Bit 7: Loss of Receive Clock Condition Clear (LORCC).

0 = interrupt masked
 1 = interrupt enabled

Bit 6: Spare Code Detected Condition Clear (LSPC).

0 = interrupt masked
 1 = interrupt enabled

Bit 5: Loop-Down Code Detected Condition Clear (LDNC).

0 = interrupt masked
 1 = interrupt enabled

Bit 4: Loop-Up Code Detected Condition Clear (LUPC).

0 = interrupt masked
 1 = interrupt enabled

Bit 3: Loss of Receive Clock Condition Detect (LORCD).

0 = interrupt masked
 1 = interrupt enabled

Bit 2: Spare Code Detected Condition Detect (LSPD).

0 = interrupt masked
 1 = interrupt enabled

Bit 1: Loop-Down Code Detected Condition Detect (LDND).

0 = interrupt masked
 1 = interrupt enabled

Bit 0: Loop-Up Code Detected Condition Detect (LUPD).

0 = interrupt masked
 1 = interrupt enabled

Register Name: **RIM3 (E1 Mode)**
 Register Description: **Receive Interrupt Mask Register 3**
 Register Address: **0A2h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|---|---------|-------|-------|---|---------|-------|
| Name | LORCC | — | V52LNKC | RDMAC | LORCD | — | V52LNKD | RDMAD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: For T1 mode, see [RIM3](#).

Bit 7: Loss of Receive Clock Clear (LORCC).

0 = interrupt masked
 1 = interrupt enabled

Bit 5: V5.2 Link Detected Clear (V52LNKC).

0 = interrupt masked
 1 = interrupt enabled

Bit 4: Receive Distant MF Alarm Clear (RDMAC).

0 = interrupt masked
 1 = interrupt enabled

Bit 3: Loss of Receive Clock Detect (LORCD).

0 = interrupt masked
 1 = interrupt enabled

Bit 1: V5.2 Link Detect (V52LNKD).

0 = interrupt masked
 1 = interrupt enabled

Bit 0: Receive Distant MF Alarm Detect (RDMAD).

0 = interrupt masked
 1 = interrupt enabled

Register Name: **RIM4**
 Register Description: **Receive Interrupt Mask Register 4**
 Register Address: **0A3h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|-------|-------|---|-------|------|-------|-----|
| Name | RESF | RESEM | RSLIP | — | RSCOS | 1SEC | TIMER | RMF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive Elastic Store Full Event (RESF).

0 = interrupt masked
 1 = interrupt enabled

Bit 6: Receive Elastic Store Empty Event (RESEM).

0 = interrupt masked
 1 = interrupt enabled

Bit 5: Receive Elastic Store Slip Occurrence Event (RSLIP).

0 = interrupt masked
 1 = interrupt enabled

Bit 3: Receive-Signaling Change-of-State Event (RSCOS).

0 = interrupt masked
 1 = interrupt enabled

Bit 2: One-Second Timer (1SEC).

0 = interrupt masked
 1 = interrupt enabled

Bit 1: Timer Event (TIMER).

0 = interrupt masked
 1 = interrupt enabled

Bit 0: Receive Multiframe Event (RMF).

0 = interrupt masked
 1 = interrupt enabled

Register Name: **RIM5**
 Register Description: **Receive Interrupt Mask Register 5 (HDLC)**
 Register Address: **0A4h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|------|-------|-----|-----|-------|------|
| Name | — | — | ROVR | RHOBT | RPE | RPS | RHWMS | RNES |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 5: Receive FIFO Overrun (ROVR).

0 = interrupt masked
 1 = interrupt enabled

Bit 4: Receive HDLC Opening Byte Event (RHOBT).

0 = interrupt masked
 1 = interrupt enabled

Bit 3: Receive Packet-End Event (RPE).

0 = interrupt masked
 1 = interrupt enabled

Bit 2: Receive Packet-Start Event (RPS).

0 = interrupt masked
 1 = interrupt enabled

Bit 1: Receive FIFO Above High Watermark Set Event (RHWMS).

0 = interrupt masked
 1 = interrupt enabled

Bit 0: Receive FIFO Not Empty Set Event (RNES).

0 = interrupt masked
 1 = interrupt enabled

Register Name: **RIM7 (T1 Mode)**
 Register Description: **Receive Interrupt Mask Register 7 (BOC:FDL)**
 Register Address: **0A6h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---------|---------|--------|-------|----|----|
| Name | — | — | RRAI-CI | RAIS-CI | RSLC96 | RFDLF | BC | BD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: For E1 mode, see [RIM7](#).

Bit 5: Receive RAI-CI (RRAI-CI).

0 = interrupt masked
 1 = interrupt enabled

Bit 4: Receive AIS-CI (RAIS-CI).

0 = interrupt masked
 1 = interrupt enabled

Bit 3: Receive SLC-96 (RSLC96).

0 = interrupt masked
 1 = interrupt enabled

Bit 2: Receive FDL Register Full (RFDLF).

0 = interrupt masked
 1 = interrupt enabled

Bit 1: BOC Clear Event (BC).

0 = interrupt masked
 1 = interrupt enabled

Bit 0: BOC Detect Event (BD).

0 = interrupt masked
 1 = interrupt enabled

Register Name: **RIM7 (E1 Mode)**
 Register Description: **Receive Interrupt Mask Register 7 (BOC:FDL)**
 Register Address: **A6h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|-------|-------|
| Name | — | — | — | — | — | — | Sa6CD | SaXCD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: For T1 mode, see [RIM7](#).

Bit 1: Sa6 Codeword Detect. This bit will enable the interrupt generated when a valid codeword (per ETS 300 233) is detected in the Sa6 bits.

0 = interrupt masked
 1 = interrupt enabled

Bit 0: SaX Change Detect. This bit will enable the interrupt generated when a change of state is detected in any of the unmasked SaX bit positions. The masked or unmasked SaX bits are selected by the [E1RSAIMR](#) register.

0 = interrupt masked
 1 = interrupt enabled

Register Name: **RSCSE1, RSCSE2, RSCSE3, RSCSE4**
 Register Description: **Receive-Signaling Change of State Enable Registers 1 to 4**
 Register Address: **0A8h, 0A9h, 0AAh, 0Abh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | (MSB) 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) | |
|---------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|---------------------------------|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | RSCSE1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | RSCSE2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | RSCSE3 |
| | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> | RSCSE4 (E1 Mode Only) |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Setting any of the CH[1:32] bits in the RSCSE1:RSCSE4 registers will cause RSCOS ([RLS4.3](#)) to be set when that channel's signaling data changes state.

Register Name: **T1RUPCD1 (T1 Mode Only)**
 Register Description: **Receive Up Code Definition Register 1**
 Register Address: **0ACh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: Writing this register resets the detector's integration period.

Bit 7: Receive Up Code Definition Bit 7 (C7). First bit of the repeating pattern.

Bit 6: Receive Up Code Definition Bit 6 (C6). A Don't Care if a 1-bit length is selected.

Bit 5: Receive Up Code Definition Bit 5 (C5). A Don't Care if a 1- or 2-bit length is selected.

Bit 4: Receive Up Code Definition Bit 4 (C4). A Don't Care if a 1- to 3-bit length is selected.

Bit 3: Receive Up Code Definition Bit 3 (C3). A Don't Care if a 1- to 4-bit length is selected.

Bit 2: Receive Up Code Definition Bit 2 (C2). A Don't Care if a 1- to 5-bit length is selected.

Bit 1: Receive Up Code Definition Bit 1 (C1). A Don't Care if a 1- to 6-bit length is selected.

Bit 0: Receive Up Code Definition Bit 0 (C0). A Don't Care if a 1- to 7-bit length is selected.

Register Name: **T1RUPCD2 (T1 Mode Only)**
 Register Description: **Receive Up Code Definition Register 2**
 Register Address: **0ADh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive Up Code Definition Bit 7 (C7). A Don't Care if a 1- to 7-bit length is selected.

Bit 6: Receive Up Code Definition Bit 6 (C6). A Don't Care if a 1- to 7-bit length is selected.

Bit 5: Receive Up Code Definition Bit 5 (C5). A Don't Care if a 1- to 7-bit length is selected.

Bit 4: Receive Up Code Definition Bit 4 (C4). A Don't Care if a 1- to 7-bit length is selected.

Bit 3: Receive Up Code Definition Bit 3 (C3). A Don't Care if a 1- to 7-bit length is selected.

Bit 2: Receive Up Code Definition Bit 2 (C2). A Don't Care if a 1- to 7-bit length is selected.

Bit 1: Receive Up Code Definition Bit 1 (C1). A Don't Care if a 1- to 7-bit length is selected.

Bit 0: Receive Up Code Definition Bit 0 (C0). A Don't Care if a 1- to 7-bit length is selected.

Register Name: **T1RDNCD1 (T1 Mode Only)**
 Register Description: **Receive Down Code Definition Register 1**
 Register Address: **0AEh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: Writing this register resets the detector's integration period.

Bit 7: Receive Down Code Definition Bit 7 (C7). First bit of the repeating pattern.

Bit 6: Receive Down Code Definition Bit 6 (C6). A Don't Care if a 1-bit length is selected.

Bit 5: Receive Down Code Definition Bit 5 (C5). A Don't Care if a 1- or 2-bit length is selected.

Bit 4: Receive Down Code Definition Bit 4 (C4). A Don't Care if a 1- to 3-bit length is selected.

Bit 3: Receive Down Code Definition Bit 3 (C3). A Don't Care if a 1- to 4-bit length is selected.

Bit 2: Receive Down Code Definition Bit 2 (C2). A Don't Care if a 1- to 5-bit length is selected.

Bit 1: Receive Down Code Definition Bit 1 (C1). A Don't Care if a 1- to 6-bit length is selected.

Bit 0: Receive Down Code Definition Bit 0 (C0). A Don't Care if a 1- to 7-bit length is selected.

Register Name: **T1RDNCD2 (T1 Mode Only)**
 Register Description: **Receive Down Code Definition Register 2**
 Register Address: **0AFh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive Down Code Definition Bit 7 (C7). A Don't Care if a 1- to 7-bit length is selected.

Bit 6: Receive Down Code Definition Bit 6 (C6). A Don't Care if a 1- to 7-bit length is selected.

Bit 5: Receive Down Code Definition Bit 5 (C5). A Don't Care if a 1- to 7-bit length is selected.

Bit 4: Receive Down Code Definition Bit 4 (C4). A Don't Care if a 1- to 7-bit length is selected.

Bit 3: Receive Down Code Definition Bit 3 (C3). A Don't Care if a 1- to 7-bit length is selected.

Bit 2: Receive Down Code Definition Bit 2 (C2). A Don't Care if a 1- to 7-bit length is selected.

Bit 1: Receive Down Code Definition Bit 1 (C1). A Don't Care if a 1- to 7-bit length is selected.

Bit 0: Receive Down Code Definition Bit 0 (C0). A Don't Care if a 1- to 7-bit length is selected.

Register Name: **RRTS1**
 Register Description: **Receive Real-Time Status Register 1**
 Register Address: **0B0h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|------|------|------|------|
| Name | — | — | — | — | RRAI | RAIS | RLOS | RLOF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are real-time (not latched).

Bit 3: Receive Remote Alarm Indication Condition (RRAI). Set when a remote alarm is received at RTIP and RRING.

Bit 2: Receive Alarm Indication Signal Condition (RAIS). Set when an unframed all-ones code is received at RTIP and RRING.

Bit 1: Receive Loss of Signal Condition (RLOS). Set when 192 consecutive zeros have been detected after the B8ZS/HDB3 decoder.

Bit 0: Receive Loss of Frame Condition (RLOF). Set when the DS26524 is not synchronized to the received data stream.

Register Name: **RRTS3 (T1 Mode)**
 Register Description: **Receive Real-Time Status Register 3**
 Register Address: **0B2h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|------|-----|-----|-----|
| Name | — | — | — | — | LORC | LSP | LDN | LUP |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are real-time (not latched). See [RRTS3](#) for E1 mode.

Bit 3: Loss of Receive Clock Condition (LORC). Set when the RCLK pin has not transitioned for one channel time.

Bit 2: Spare Code Detected Condition (LSP). Set when the spare code as defined in the [T1RSCD1:T1RSCD2](#) registers is being received.

Bit 1: Loop-Down Code Detected Condition (LDN). Set when the loop-down code as defined in the [T1RDNCD1:T1RDNCD2](#) register is being received.

Bit 0: Loop-Up Code Detected Condition (LUP). Set when the loop-up code as defined in the [T1RUPCD1:T1RUPCD2](#) register is being received.

Register Name: **RRTS3 (E1 Mode)**
 Register Description: **Receive Real-Time Status Register 3**
 Register Address: **0B2h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|------|---|--------|------|
| Name | — | — | — | — | LORC | — | V52LNK | RDMA |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are real-time (not latched). See [RRTS3](#) for T1 mode.

Bit 3: Loss of Receive Clock Condition (LORC). Set when the RCLK pin has not transitioned for one channel time.

Bit 1: V5.2 Link Detected Condition (V52LNK). Set on detection of a V5.2 link identification signal (G.965).

Bit 0: Receive Distant MF Alarm Condition (RDMA). Set when bit 6 of time slot 16 in frame 0 has been set for two consecutive multiframes. This alarm is not disabled in the CCS signaling mode.

Register Name: **RRTS5**
 Register Description: **Receive Real-Time Status Register 5 (HDLC)**
 Register Address: **0B4h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|-----|-----|-----|---|---|------|-----|
| Name | — | PS2 | PS1 | PS0 | — | — | RHWM | RNE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are real time.

Bits 6 to 4: Receive Packet Status (PS[2:0]). These are real-time bits indicating the status as of the last read of the receive FIFO.

| PS2 | PS1 | PS0 | PACKET STATUS |
|-----|-----|-----|--|
| 0 | 0 | 0 | In Progress: End of message has not yet been reached. |
| 0 | 0 | 1 | Packet OK: Packet ended with correct CRC codeword. |
| 0 | 1 | 0 | CRC Error: A closing flag was detected, preceded by a corrupt CRC codeword. |
| 0 | 1 | 1 | Abort: Packet ended because an abort signal was detected (7 or more ones in a row). |
| 1 | 0 | 0 | Overrun: HDLC controller terminated reception of packet because receive FIFO is full. |

Bit 1: Receive FIFO Above High Watermark Condition (RHWM). Set when the receive 64-byte FIFO fills beyond the high watermark as defined by the Receive HDLC FIFO Control register (RHFC). This is a real-time bit.

Bit 0: Receive FIFO Not Empty Condition (RNE). Set when the receive 64-byte FIFO has at least one byte available for a read. This is a real-time bit.

Register Name: **RHPBA**
 Register Description: **Receive HDLC Packet Bytes Available Register**
 Register Address: **0B5h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|-------|-------|-------|-------|-------|-------|-------|
| Name | MS | RPBA6 | RPBA5 | RPBA4 | RPBA3 | RPBA2 | RPBA1 | RPBA0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Message Status (MS).

0 = Bytes indicated by RPBA[6:0] are the end of a message. Host must check the HDLC status register for details.

1 = Bytes indicated by RPBA[6:0] are the beginning or continuation of a message. The host does not need to check the HDLC status. The MS bit returns to a value of 1 when the Rx HDLC FIFO is empty.

Bits 6 to 0: Receive FIFO Packet Bytes Available Count (RPBA[6:0]). RPBA0 is the LSB.

Register Name: **RHF**
 Register Description: **Receive HDLC FIFO Register**
 Register Address: **0B6h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | RHD7 | RHD6 | RHD5 | RHD4 | RHD3 | RHD2 | RHD1 | RHD0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive HDLC Data Bit 7 (RHD7). MSB of a HDLC packet data byte.

Bit 6: Receive HDLC Data Bit 6 (RHD6).

Bit 5: Receive HDLC Data Bit 5 (RHD5).

Bit 4: Receive HDLC Data Bit 4 (RHD4).

Bit 3: Receive HDLC Data Bit 3 (RHD3).

Bit 2: Receive HDLC Data Bit 2 (RHD2).

Bit 1: Receive HDLC Data Bit 1 (RHD1).

Bit 0: Receive HDLC Data Bit 0 (RHD0). LSB of a HDLC packet data byte.

Register Name: **RBCS1, RBCS2, RBCS3, RBCS4**
 Register Description: **Receive Blank Channel Select Registers 1 to 4**
 Register Address: **0C0h, 0C1h, 0C2h, 0C3h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---------|------|------|------|------|------|------|------|------|---|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | RBCS1 RBCS2 RBCS3 RBCS4 (E1 Mode Only) |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | |
| | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Bit 7 to 0: Receive Blank Channel Select for Channels 1 to 32 (CH[1:32]).

0 = Do not blank this channel (channel data is available on RSER)

1 = Data on RSER is forced to all ones for this channel

Note that when two or more sequential channels are chosen to be blanked, the receive-slip zone select bit should be set to 0. If the blank channels are distributed (such as 1, 5, 9, 13, 17, 21, 25, 29), the RSZS bit can be set to 1, which may provide a lower occurrence of slips in certain applications.

Register Name: **RCBR1, RCBR2, RCBR3, RCBR4**
 Register Description: **Receive Channel Blocking Registers 1 to 4**
 Register Address: **0C4h, 0C5h, 0C6h, 0C7h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|---------------------|----------------------------------|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | RCBR1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | RCBR2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | RCBR3 |
| | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25 (F-bit)</i> | RCBR4* (E1 Mode Only) |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Bits 7 to 0: Receive Channel Blocking Control Bits for Channels 1 to 32 (CH[1:32]).

0 = force the RCHBLK pin to remain low during this channel time

1 = force the RCHBLK pin high during this channel time

***Note that RCBR4 has two functions:**

When 2.048MHz backplane mode is selected, this register allows the user to enable the channel blocking signal for any of the 32 possible backplane channels.

When 1.544MHz backplane mode is selected, the LSB of this register determines whether or not the RCHBLK signal will pulse high during the F-Bit time. In this mode, [RCBR4.1:RCBR4.7](#) should be set to 0.

[RCBR4.0](#) = 0, do not pulse RCHBLK during the F-bit.

[RCBR4.0](#) = 1, pulse RCHBLK during the F-bit.

Register Name: **RSI1, RSI2, RSI3, RSI4**
 Register Description: **Receive-Signaling Reinsertion Enable Registers 1 to 4**
 Register Address: **0C8h, 0C9h, 0CAh, 0CBh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|--------------------------------|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | RSI1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | RSI2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | RSI3 |
| | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> | RSI4 (E1 Mode Only) |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Setting any of the CH[1:24] bits in the RSI1:RSI3 registers causes signaling data to be reinserted for the associated channel. RSI4 is used for 2.048MHz backplane operation.

Register Name: **RGCCS1, RGCCS2, RGCCS3, RGCCS4**
 Register Description: **Receive Gapped-Clock Channel Select Registers 1 to 4**
 Register Address: **0CCh, 0CDh, 0CEh, 0CFh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---------|------|------|------|------|------|------|------|-----------------|---|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | RGCCS1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | RGCCS2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | RGCCS3 |
| | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 (F-bit) | RGCCS4* (E1 Mode Only) |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Bits 7 to 0: Receive Gapped Clock Channel Select Bits for Channels 1 to 32 (CH[1:32]).

0 = no clock is present on RCHCLK during this channel time

1 = force a clock on RCHCLK during this channel time. The clock will be synchronous with RCLK if the elastic store is disabled, and synchronous with RSYSCLK if the elastic store is enabled.

***Note that RGCCS4 has two functions:**

When 2.048MHz backplane mode is selected, this register allows the user to enable the gapped clock on RCHCLK for any of the 32 possible backplane channels.

When 1.544MHz backplane mode is selected, the LSB of this register determines whether or not a clock is generated on RCHCLK during the F-bit time:

RGCCS4.0 = 0, do not generate a clock during the F-bit.

RGCCS4.0 = 1, generate a clock during the F-bit.

In this mode, RGCCS4.1:RGCCS4.7 should be set to 0.

Register Name: **RCICE1, RCICE2, RCICE3, RCICE4**
 Register Description: **Receive Channel Idle Code Enable Registers 1 to 4**
 Register Address: **0D0h, 0D1h, 0D2h, 0D3h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | (MSB) 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) | |
|---------|---------|------|------|------|------|------|------|---------|--|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | RCICE1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | RCICE2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | RCICE3 |
| | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | RCICE4 (E1 Mode Only) |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Bits 7 to 0: Receive Channel Idle Code Insertion Control Bits for Channels 1 to 32 (CH[1:32]).

0 = do not insert data from the Idle Code Array into the receive data stream

1 = insert data from the Idle Code Array into the receive data stream

Register Name: **RBPCS1, RBPCS2, RBPCS3, RBPCS4**
 Register Description: **Receive BERT Port Channel Select Registers 1 to 4**
 Register Address: **0D4h, 0D5h, 0D6h, 0D7h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | (MSB) 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) | |
|---------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|----------------------------------|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | RBPCS1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | RBPCS2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | RBPCS3 |
| | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> | RBPCS4 (E1 Mode Only) |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Bits 7 to 0: BERT Port Channel Select Receive Channels 1 to 32 (CH[1:32]).

0 = Do not enable the receive BERT clock for the associated channel time, or map the selected channel data out of the receive BERT port.

1 = Enable the receive BERT clock for the associated channel time, and allow mapping of the selected channel data out of the receive BERT port. Multiple or all channels may be selected simultaneously.

9.4.2 Transmit Register Definitions

Register Name: **THC1**
 Register Description: **Transmit HDLC Control Register 1**
 Register Address: **110h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|-------|-----|------|-----|------|------|-------|
| Name | NOFS | TEOML | THR | THMS | TFS | TEOM | TZSD | TCRCD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Number of Flags Select (NOFS).

- 0 = send one flag between consecutive messages
- 1 = send two flags between consecutive messages

Bit 6: Transmit End of Message and Loop (TEOML). To loop on a message, this bit should be set to a one just before the last data byte of an HDLC packet is written into the transmit FIFO. The message will repeat until the user clears this bit or a new message is written to the transmit FIFO. If the host clears the bit, the looping message will complete then flags will be transmitted until new message is written to the FIFO. If the host terminates the loop by writing a new message to the FIFO the loop will terminate, one or two flags will be transmitted and the new message will start. If not disabled via TCRCD, the transmitter will automatically append a 2-byte CRC code to the end of all messages.

Bit 5: Transmit HDLC Reset (THR). Will reset the transmit HDLC controller and flush the transmit FIFO. An abort followed by 7Eh or FFh flags/idle will be transmitted until a new packet is initiated by writing new data into the FIFO. This is an acknowledged reset, that is, the host need only to set the bit and the DS26524 will clear it once the reset operation is complete. Total time for the reset is less than 250µs.

- 0 = Normal operation
- 1 = Reset transmit HDLC controller and flush the transmit FIFO

Bit 4: Transmit HDLC Mapping Select (THMS).

- 0 = Transmit HDLC assigned to channels
- 1 = Transmit HDLC assigned to FDL (T1 mode), Sa bits (E1 mode). This mode must be enabled with [TCR2.7](#).

Bit 3: Transmit Flag/Idle Select (TFS). This bit selects the inter-message fill character after the closing and before the opening flags (7Eh).

- 0 = 7Eh
- 1 = FFh

Bit 2: Transmit End of Message (TEOM). Should be set to a one just before the last data byte of an HDLC packet is written into the transmit FIFO at THF. If not disabled via TCRCD, the transmitter will automatically append a 2-byte CRC code to the end of the message.

Bit 1: Transmit Zero Stuffer Defeat (TZSD). The zero stuffer function automatically inserts a zero in the message field (between the flags) after five consecutive ones to prevent the emulation of a flag or abort sequence by the data pattern. The receiver automatically removes (destuffs) any zero after five ones in the message field.

- 0 = enable the zero stuffer (normal operation)
- 1 = disable the zero stuffer

Bit 0: Transmit CRC Defeat (TCRCD). A 2-byte CRC code is automatically appended to the outbound message. This bit can be used to disable the CRC function.

- 0 = enable CRC generation (normal operation)
- 1 = disable CRC generation

Register Name: **THBSE**
 Register Description: **Transmit HDLC Bit Suppress Register**
 Register Address: **111h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | TBSE8 | TBSE7 | TBSE6 | TBSE5 | TBSE4 | TBSE3 | TBSE2 | TBSE1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit Bit 8 Suppress (TBSE8). MSB of the channel. Set to one to stop this bit from being used.

Bit 6: Transmit Bit 7 Suppress (TBSE7). Set to one to stop this bit from being used.

Bit 5: Transmit Bit 6 Suppress (TBSE6). Set to one to stop this bit from being used.

Bit 4: Transmit Bit 5 Suppress (TBSE5). Set to one to stop this bit from being used.

Bit 3: Transmit Bit 4 Suppress (TBSE4). Set to one to stop this bit from being used.

Bit 2: Transmit Bit 3 Suppress (TBSE3). Set to one to stop this bit from being used.

Bit 1: Transmit Bit 2 Suppress (TBSE2). Set to one to stop this bit from being used.

Bit 0: Transmit Bit 1 Suppress (TBSE1). LSB of the channel. Set to one to stop this bit from being used.

Register Name: **THC2**
 Register Description: **Transmit HDLC Control Register 2**
 Register Address: **113h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|------|--------------|--------------|--------------|--------------|--------------|--------------|
| Name | TABT | SBOC | THCEN | THCS4 | THCS3 | THCS2 | THCS1 | THCS0 |
| | <i>TABT</i> | — | <i>THCEN</i> | <i>THCS4</i> | <i>THCS3</i> | <i>THCS2</i> | <i>THCS1</i> | <i>THCS0</i> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit Abort (TABT). A 0-to-1 transition will cause the FIFO contents to be dumped and one FEh abort to be sent followed by 7Eh or FFh flags/idle until a new packet is initiated by writing new data into the FIFO. Must be cleared and set again for a subsequent abort to be sent.

Bit 6: Send BOC (SBOC) (T1 Mode Only). Set = 1 to transmit the BOC code placed in bits 0 to 5 of the [T1TBOC](#) register.

Bit 5: Transmit HDLC Controller Enable (THCEN).

0 = Transmit HDLC controller is not enabled.

1 = Transmit HDLC controller is enabled.

Bits 4 to 0: Transmit HDLC Channel Select (THCS[4:0]). Determines which DSO channel will carry the HDLC message if enabled. Changes to this value are acknowledged only upon a transmit HDLC controller reset (THR at [THC1.5](#)).

Register Name: **E1TSACR (E1 Mode)**
 Register Description: **E1 Transmit Sa-Bit Control Register**
 Register Address: **114h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|-------|----|-----|-----|-----|-----|-----|
| Name | SiAF | SiNAF | RA | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: International Bit in Align Frame Insertion Control Bit (SiAF).

0 = do not insert data from the TSiAF register into the transmit data stream
 1 = insert data from the TSiAF register into the transmit data stream

Bit 6: International Bit in Non-Align Frame Insertion Control Bit (SiNAF).

0 = do not insert data from the TSiNAF register into the transmit data stream
 1 = insert data from the TSiNAF register into the transmit data stream

Bit 5: Remote Alarm Insertion Control Bit (RA).

0 = do not insert data from the TRA register into the transmit data stream
 1 = insert data from the TRA register into the transmit data stream

Bit 4: Additional Bit 4 Insertion Control Bit (Sa4).

0 = do not insert data from the TSa4 register into the transmit data stream
 1 = insert data from the TSa4 register into the transmit data stream

Bit 3: Additional Bit 5 Insertion Control Bit (Sa5).

0 = do not insert data from the TSa5 register into the transmit data stream
 1 = insert data from the TSa5 register into the transmit data stream

Bit 2: Additional Bit 6 Insertion Control Bit (Sa6).

0 = do not insert data from the TSa6 register into the transmit data stream
 1 = insert data from the TSa6 register into the transmit data stream

Bit 1: Additional Bit 7 Insertion Control Bit (Sa7).

0 = do not insert data from the TSa7 register into the transmit data stream
 1 = insert data from the TSa7 register into the transmit data stream

Bit 0: Additional Bit 8 Insertion Control Bit (Sa8).

0 = do not insert data from the TSa8 register into the transmit data stream
 1 = insert data from the TSa8 register into the transmit data stream

Register Name: **SSIE1, SSIE2, SSIE3, SSIE4**
 Register Description: **Software-Signaling Insertion Enable Registers 1 to 4**
 Register Address: **118h, 119h, 11Ah, 11Bh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | (MSB) 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) | |
|---------|---------|------|------|------|------|------|------|---------|---|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | SSIE1 SSIE2 SSIE3 SSIE4 (E1 Mode Only) |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | |
| | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Bits 7 to 0: Software Signaling Insertion Enable for Channels 1 to 32 (CH[1:32]). These bits determine which channels are to have signaling inserted from the transmit-signaling registers.

0 = do not source signaling data from the TS registers for this channel

1 = source signaling data from the TS registers for this channel

Register Name: **TIDR1 to TIDR32**
 Register Description: **Transmit Idle Code Definition Registers 1 to 32**
 Register Address: **120h to 13Fh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Per-Channel Idle Code Bits (C[7:0]). C0 is the LSB of the code (this bit is transmitted last). Address 120h is for channel 1, address 13Fh is for channel 32. TIDR1:TIDR24 are T1 mode. TIDR25:TIDR32 are E1 mode.

Register Name: **TS1 to TS16**
 Register Description: **Transmit-Signaling Registers 1 to 16**
 Register Address: **140h to 14Fh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

T1 Mode:

| Bit # | (MSB) 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) | |
|-------|---------|--------|--------|--------|--------|--------|--------|---------|------|
| Name | CH1-A | CH1-B | CH1-C | CH1-D | CH13-A | CH13-B | CH13-C | CH13-D | TS1 |
| | CH2-A | CH2-B | CH2-C | CH2-D | CH14-A | CH14-B | CH14-C | CH14-D | TS2 |
| | CH3-A | CH3-B | CH3-C | CH3-D | CH15-A | CH15-B | CH15-C | CH15-D | TS3 |
| | CH4-A | CH4-B | CH4-C | CH4-D | CH16-A | CH16-B | CH16-C | CH16-D | TS4 |
| | CH5-A | CH5-B | CH5-C | CH5-D | CH17-A | CH17-B | CH17-C | CH17-D | TS5 |
| | CH6-A | CH6-B | CH6-C | CH6-D | CH18-A | CH18-B | CH18-C | CH18-D | TS6 |
| | CH7-A | CH7-B | CH7-C | CH7-D | CH19-A | CH19-B | CH19-C | CH19-D | TS7 |
| | CH8-A | CH8-B | CH8-C | CH8-D | CH20-A | CH20-B | CH20-C | CH20-D | TS8 |
| | CH9-A | CH9-B | CH9-C | CH9-D | CH21-A | CH21-B | CH21-C | CH21-D | TS9 |
| | CH10-A | CH10-B | CH10-C | CH10-D | CH22-A | CH22-B | CH22-C | CH22-D | TS10 |
| | CH11-A | CH11-B | CH11-C | CH11-D | CH23-A | CH23-B | CH23-C | CH23-D | TS11 |
| | CH12-A | CH12-B | CH12-C | CH12-D | CH24-A | CH24-B | CH24-C | CH24-D | TS12 |

Note: In D4 framing mode, the C and D bits are not used.

E1 Mode:

| Bit # | (MSB) 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) | |
|-------|---------|--------|--------|--------|--------|--------|--------|---------|------|
| Name | 0 | 0 | 0 | 0 | X | Y | X | X | TS1 |
| | CH1-A | CH1-B | CH1-C | CH1-D | CH16-A | CH16-B | CH16-C | CH16-D | TS2 |
| | CH2-A | CH2-B | CH2-C | CH2-D | CH17-A | CH17-B | CH17-C | CH17-D | TS3 |
| | CH3-A | CH3-B | CH3-C | CH3-D | CH18-A | CH18-B | CH18-C | CH18-D | TS4 |
| | CH4-A | CH4-B | CH4-C | CH4-D | CH19-A | CH19-B | CH19-C | CH19-D | TS5 |
| | CH5-A | CH5-B | CH5-C | CH5-D | CH20-A | CH20-B | CH20-C | CH20-D | TS6 |
| | CH6-A | CH6-B | CH6-C | CH6-D | CH21-A | CH21-B | CH21-C | CH21-D | TS7 |
| | CH7-A | CH7-B | CH7-C | CH7-D | CH22-A | CH22-B | CH22-C | CH22-D | TS8 |
| | CH8-A | CH8-B | CH8-C | CH8-D | CH23-A | CH23-B | CH23-C | CH23-D | TS9 |
| | CH9-A | CH9-B | CH9-C | CH9-D | CH24-A | CH24-B | CH24-C | CH24-D | TS10 |
| | CH10-A | CH10-B | CH10-C | CH10-D | CH25-A | CH25-B | CH25-C | CH25-D | TS11 |
| | CH11-A | CH11-B | CH11-C | CH11-D | CH26-A | CH26-B | CH26-C | CH26-D | TS12 |
| | CH12-A | CH12-B | CH12-C | CH12-D | CH27-A | CH27-B | CH27-C | CH27-D | TS13 |
| | CH13-A | CH13-B | CH13-C | CH13-D | CH28-A | CH28-B | CH28-C | CH28-D | TS14 |
| | CH14-A | CH14-B | CH14-C | CH14-D | CH29-A | CH29-B | CH29-C | CH29-D | TS15 |
| | CH15-A | CH15-B | CH15-C | CH15-D | CH30-A | CH30-B | CH30-C | CH30-D | TS16 |

Register Name: **TCICE1, TCICE2, TCICE3, TCICE4**
 Register Description: **Transmit Channel Idle Code Enable Registers 1 to 4**
 Register Address: **150h, 151h, 152h, 153h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | (MSB) 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) | |
|---------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|--------------------------|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | TCICE1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | TCICE2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | TCICE3 |
| | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> | TCICE4 (E1 Mode Only) |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

The Transmit Channel Idle Code Enable registers (TCICE1:TCICE4) are used to determine which of the 24 T1 channels (or 32 E1 channels) from the backplane should be overwritten with the code placed in the Transmit Idle Code Definition register ([TIDR1](#):TIDR32).

Bits 7 to 0: Transmit Channels 1 to 32 Code Insertion Control Bits (CH[1:32]).

0 = do not insert data from the Idle Code Array into the transmit data stream

1 = insert data from the Idle Code Array into the transmit data stream

Register Name: **TFRID**
 Register Description: **Transmit Firmware Revision ID Register**
 Register Address: **161h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | FR7 | FR6 | FR5 | FR4 | FR3 | FR2 | FR1 | FR0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Firmware Revision (FR[7:0]). This read-only register reports the transmitter firmware revision.

Register Name: **T1TFDL (T1 Mode)**
 Register Description: **Transmit FDL Register**
 Register Address: **162h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | TFDL7 | TFDL6 | TFDL5 | TFDL4 | TFDL3 | TFDL2 | TFDL1 | TFDL0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: Also used to insert Fs framing pattern in D4 framing mode.

The Transmit FDL register (T1TFDL) contains the Facility Data Link (FDL) information that is to be inserted on a byte basis into the outgoing T1 data stream. The LSB is transmitted first. In D4 mode, only the lower six bits are used.

Bit 7: Transmit FDL Bit 7 (TFDL7). MSB of the transmit FDL code.

Bit 6: Transmit FDL Bit 6 (TFDL6).

Bit 5: Transmit FDL Bit 5 (TFDL5).

Bit 4: Transmit FDL Bit 4 (TFDL4).

Bit 3: Transmit FDL Bit 3 (TFDL3).

Bit 2: Transmit FDL Bit 2 (TFDL2).

Bit 1: Transmit FDL Bit 1 (TFDL1).

Bit 0: Transmit FDL Bit 0 (TFDL0). LSB of the transmit FDL code.

Register Name: **T1TBOC (T1 Mode Only)**
 Register Description: **Transmit BOC Register**
 Register Address: **163h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|-------|-------|-------|-------|-------|-------|
| Name | — | — | TBOC5 | TBOC4 | TBOC3 | TBOC2 | TBOC1 | TBOC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 5: Transmit BOC Bit 5 (TBOC5). MSB of the transmit BOC code.

Bit 4: Transmit BOC Bit 4 (TBOC4).

Bit 3: Transmit BOC Bit 3 (TBOC3).

Bit 2: Transmit BOC Bit 2 (TBOC2).

Bit 1: Transmit BOC Bit 1 (TBOC1).

Bit 0: Transmit BOC Bit 0 (TBOC0). LSB of the transmit BOC code.

Register Name: **T1TSLC1, T1TSLC2, T1TSLC3 (T1 Mode)**
 Register Description: **Transmit SLC-96 Data Link Registers 1 to 3**
 Register Address: **164h, 165h, 166h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | (MSB) 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) | |
|---------|---------|----|-----|-----|-----|-----|-----|---------|---------|
| Name | C8 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | T1TSLC1 |
| | M2 | M1 | S=0 | S=1 | S=0 | C11 | C10 | C9 | T1TSLC2 |
| | S=1 | S4 | S3 | S2 | S1 | A2 | A1 | M3 | T1TSLC3 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Note: See [E1TAF](#), [E1TNAF](#), and [E1TSlAF](#) for E1 modes.

Register Name: **E1TAF (E1 Mode)**
 Register Description: **Transmit Align Frame Register**
 Register Address: **164h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|---|---|---|---|---|---|---|
| Name | Si | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Default | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |

Bit 7: International Bit (Si).

Bit 6: Frame Alignment Signal Bit (0).

Bit 5: Frame Alignment Signal Bit (0).

Bit 4: Frame Alignment Signal Bit (1).

Bit 3: Frame Alignment Signal Bit (1).

Bit 2: Frame Alignment Signal Bit (0).

Bit 1: Frame Alignment Signal Bit (1).

Bit 0: Frame Alignment Signal Bit (1).

Register Name: **E1TNAF (E1 Mode)**
 Register Description: **Transmit Non-Align Frame Register**
 Register Address: **165h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|---|---|-----|-----|-----|-----|-----|
| Name | Si | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| Default | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: International Bit (Si).

Bit 6: Frame Non-Alignment Signal Bit (1).

Bit 5: Remote Alarm (Used to Transmit the Alarm) (A).

Bit 4: Additional Bit 4 (Sa4).

Bit 3: Additional Bit 5 (Sa5).

Bit 2: Additional Bit 6 (Sa6).

Bit 1: Additional Bit 7 (Sa7).

Bit 0: Additional Bit 8 (Sa8).

Register Name: **E1TSiAF (E1 Mode)**
 Register Description: **Transmit Si Bits of the Align Frame Register**
 Register Address: **166h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|-------|-------|-------|-------|-------|
| Name | TSiF14 | TSiF12 | TSiF10 | TSiF8 | TSiF6 | TSiF4 | TSiF2 | TSiF0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Si Bit of Frame 14 (TSiF14).

Bit 6: Si Bit of Frame 12 (TSiF12).

Bit 5: Si Bit of Frame 10 (TSiF10).

Bit 4: Si Bit of Frame 8 (TSiF8).

Bit 3: Si Bit of Frame 6 (TSiF6).

Bit 2: Si Bit of Frame 4 (TSiF4).

Bit 1: Si Bit of Frame 2 (TSiF2).

Bit 0: Si Bit of Frame 0 (TSiF0).

Register Name: **E1TSiNAF (E1 Mode Only)**
 Register Description: **Transmit Si Bits of the Non-Align Frame Register**
 Register Address: **167h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|-------|-------|-------|-------|-------|
| Name | TSiF15 | TSiF13 | TSiF11 | TSiF9 | TSiF7 | TSiF5 | TSiF3 | TSiF1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Si Bit of Frame 15 (TSiF15).

Bit 6: Si Bit of Frame 13 (TSiF13).

Bit 5: Si Bit of Frame 11 (TSiF11).

Bit 4: Si Bit of Frame 9 (TSiF9).

Bit 3: Si Bit of Frame 7 (TSiF7).

Bit 2: Si Bit of Frame 5 (TSiF5).

Bit 1: Si Bit of Frame 3 (TSiF3).

Bit 0: Si Bit of Frame 1 (TSiF1).

Register Name: **E1TRA (E1 Mode Only)**
 Register Description: **Transmit Remote Alarm Register**
 Register Address: **168h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|-------|-------|-------|-------|-------|
| Name | TRAF15 | TRAF13 | TRAF11 | TRAF9 | TRAF7 | TRAF5 | TRAF3 | TRAF1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Remote Alarm Bit of Frame 15 (TRAF15).

Bit 6: Remote Alarm Bit of Frame 13 (TRAF13).

Bit 5: Remote Alarm Bit of Frame 11 (TRAF11).

Bit 4: Remote Alarm Bit of Frame 9 (TRAF9).

Bit 3: Remote Alarm Bit of Frame 7 (TRAF7).

Bit 2: Remote Alarm Bit of Frame 5 (TRAF5).

Bit 1: Remote Alarm Bit of Frame 3 (TRAF3).

Bit 0: Remote Alarm Bit of Frame 1 (TRAF1).

Register Name: **E1TSa4 (E1 Mode Only)**
 Register Description: **Transmit Sa4 Bits Register**
 Register Address: **169h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|--------|--------|--------|--------|--------|
| Name | TSa4F15 | TSa4F13 | TSa4F11 | TSa4F9 | TSa4F7 | TSa4F5 | TSa4F3 | TSa4F1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa4 Bit of Frame 15 (TSa4F15).

Bit 6: Sa4 Bit of Frame 13 (TSa4F13).

Bit 5: Sa4 Bit of Frame 11 (TSa4F11).

Bit 4: Sa4 Bit of Frame 9 (TSa4F9).

Bit 3: Sa4 Bit of Frame 7 (TSa4F7).

Bit 2: Sa4 Bit of Frame 5 (TSa4F5).

Bit 1: Sa4 Bit of Frame 3 (TSa4F3).

Bit 0: Sa4 Bit of Frame 1 (TSa4F1).

Register Name: **E1TSa5 (E1 Mode Only)**
 Register Description: **Transmit Sa5 Bits Register**
 Register Address: **16Ah + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|--------|--------|--------|--------|--------|
| Name | TSa5F15 | TSa5F13 | TSa5F11 | TSa5F9 | TSa5F7 | TSa5F5 | TSa5F3 | TSa5F1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa5 Bit of Frame 15 (TSa5F15).

Bit 6: Sa5 Bit of Frame 13 (TSa5F13).

Bit 5: Sa5 Bit of Frame 11 (TSa5F11).

Bit 4: Sa5 Bit of Frame 9 (TSa5F9).

Bit 3: Sa5 Bit of Frame 7 (TSa5F7).

Bit 2: Sa5 Bit of Frame 5 (TSa5F5).

Bit 1: Sa5 Bit of Frame 3 (TSa5F3).

Bit 0: Sa5 Bit of Frame 1 (TSa5F1).

Register Name: **E1TSa6 (E1 Mode)**
 Register Description: **Transmit Sa6 Bits Register**
 Register Address: **16Bh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|--------|--------|--------|--------|--------|
| Name | TSa6F15 | TSa6F13 | TSa6F11 | TSa6F9 | TSa6F7 | TSa6F5 | TSa6F3 | TSa6F1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa6 Bit of Frame 15 (TSa6F15).

Bit 6: Sa6 Bit of Frame 13 (TSa6F13).

Bit 5: Sa6 Bit of Frame 11 (TSa6F11).

Bit 4: Sa6 Bit of Frame 9 (TSa6F9).

Bit 3: Sa6 Bit of Frame 7 (TSa6F7).

Bit 2: Sa6 Bit of Frame 5 (TSa6F5).

Bit 1: Sa6 Bit of Frame 3 (TSa6F3).

Bit 0: Sa6 Bit of Frame 1 (TSa6F1).

Register Name: **E1TSa7 (E1 Mode Only)**
 Register Description: **Transmit Sa7 Bits Register**
 Register Address: **16Ch + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|--------|--------|--------|--------|--------|
| Name | TSa7F15 | TSa7F13 | TSa7F11 | TSa7F9 | TSa7F7 | TSa7F5 | TSa7F3 | TSa7F1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa7 Bit of Frame 15 (TSa7F15).

Bit 6: Sa7 Bit of Frame 13 (TSa7F13).

Bit 5: Sa7 Bit of Frame 11 (TSa7F11).

Bit 4: Sa7 Bit of Frame 9 (TSa7F9).

Bit 3: Sa7 Bit of Frame 7 (TSa7F7).

Bit 2: Sa7 Bit of Frame 5 (TSa7F5).

Bit 1: Sa7 Bit of Frame 3 (TSa7F3).

Bit 0: Sa7 Bit of Frame 1 (TSa7F1).

Register Name: **E1TSa8 (E1 Mode Only)**
 Register Description: **Transmit Sa8 Bits Register**
 Register Address: **16Dh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|--------|--------|--------|--------|--------|
| Name | TSa8F15 | TSa8F13 | TSa8F11 | TSa8F9 | TSa8F7 | TSa8F5 | TSa8F3 | TSa8F1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa8 Bit of Frame 15 (TSa8F15).

Bit 6: Sa8 Bit of Frame 13 (TSa8F13).

Bit 5: Sa8 Bit of Frame 11 (TSa8F11).

Bit 4: Sa8 Bit of Frame 9 (TSa8F9).

Bit 3: Sa8 Bit of Frame 7 (TSa8F7).

Bit 2: Sa8 Bit of Frame 5 (TSa8F5).

Bit 1: Sa8 Bit of Frame 3 (TSa8F3).

Bit 0: Sa8 Bit of Frame 1 (TSa8F1).

Register Name: **TMMR**
 Register Description: **Transmit Master Mode Register**
 Register Address: **180h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|-----------|---|---|---|---|--------|-------|
| Name | FRM_EN | INIT_DONE | — | — | — | — | SFTRST | T1/E1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Framer Enable (FRM_EN). This bit must be set to the desired state before writing INIT_DONE.
 0 = Framer disabled—held in low-power state
 1 = Framer enabled—all features active

Bit 6: Initialization Done (INIT_DONE). The user must set this bit once he has written the configuration registers. The host is required to write or clear all device registers prior to setting this bit. Once INIT_DONE is set, the DS26524 will check the FRM_EN bit and, if enabled will begin operation based on the initial configuration.

Bit 1: Soft Reset (SFTRST). Level sensitive-soft reset. Should be taken high then low to reset the transceiver.
 0 = Normal operation
 1 = Reset the transceiver

Bit 0: Transmitter T1/E1 Mode Select (T1/E1). Sets operating mode for transmitter only! This bit must be written with the desired value prior to setting INIT_DONE.
 0 = T1 operation
 1 = E1 operation

Register Name: **TCR1 (T1 Mode)**
 Register Description: **Transmit Control Register 1**
 Register Address: **181h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|------|------|------|------|-------|------|------|
| Name | TJC | TFPT | TCPT | TSSE | GB7S | TB8ZS | TAIS | TRAI |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: See [TCR1](#) for E1 mode.

Bit 7: Transmit Japanese CRC-6 Enable (TJC).

- 0 = use ANSI/AT&T:ITU-T CRC-6 calculation (normal operation)
- 1 = use Japanese standard JT-G704 CRC-6 calculation

Bit 6: Transmit F-Bit Pass Through (TFPT).

- 0 = F-bits sourced internally
- 1 = F-bits sampled at TSER

Bit 5: Transmit CRC Pass Through (TCPT).

- 0 = source CRC-6 bits internally
- 1 = CRC-6 bits sampled at TSER during F-bit time

Bit 4: Transmit Software-Signaling Enable (TSSE). This function is enabled by TB7ZS ([TCR2.0](#)).

- 0 = do not source signaling data from the TSx registers regardless of the SSIEx registers. The SSIEx registers still define which channels are to have B7 stuffing performed.
- 1 = source signaling data as enabled by the SSIEx registers.

Bit 3: Global Bit 7 Stuffing (GB7S). This function is enabled by TB7ZS ([TCR2.0](#)).

- 0 = allow the SSIEx registers to determine which channels containing all zeros are to be bit 7 stuffed
- 1 = force bit 7 stuffing in all zero-byte channels of that port, regardless of how the SSIEx registers are programmed

Bit 2: Transmit B8ZS Enable (TB8ZS).

- 0 = B8ZS disabled
- 1 = B8ZS enabled

Bit 1: Transmit Alarm Indication Signal (TAIS).

- 0 = transmit data normally
- 1 = transmit an unframed all-ones code at TPOS and TNEG

Bit 0: Transmit Remote Alarm Indication (TRAI).

- 0 = do not transmit remote alarm
- 1 = transmit remote alarm

Register Name: **TCR1 (E1 Mode)**
 Register Description: **Transmit Control Register 1**
 Register Address: **181h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|-------|------|------|-------|------|-------|
| Name | TTPT | T16S | TG802 | TSiS | TSA1 | THDB3 | TAIS | TCRC4 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: See [TCR1](#) for T1 mode.

Bit 7: Transmit Time Slot 0 Pass Through (TTPT).

0 = FAS bits/Sa bits/remote alarm sourced internally from the [E1TAF](#) and [E1TNAF](#) registers
 1 = FAS bits/Sa bits/remote alarm sourced from TSER

Bit 6: Transmit Time Slot 16 Data Select (T16S). See Section [8.9.4](#) on software signaling.

0 = time slot 16 determined by the SSiEx and [THSCS1:THSCS4](#) registers
 1 = source time slot 16 from [TS1](#):TS16 registers

Bit 5: Transmit G.802 Enable (TG802). See Section [10.4](#).

0 = do not force TCHBLK high during bit 1 of time slot 26
 1 = force TCHBLK high during bit 1 of time slot 26

Bit 4: Transmit International Bit Select (TSiS).

0 = sample Si bits at TSER pin
 1 = source Si bits from [E1TAF](#) and [E1TNAF](#) registers (in this mode, TCR1.7 must be set to 0)

Bit 3: Transmit-Signaling All Ones (TSA1).

0 = normal operation
 1 = force time slot 16 in every frame to all ones

Bit 2: Transmit HDB3 Enable (THDB3).

0 = HDB3 disabled
 1 = HDB3 enabled

Bit 1: Transmit AIS (TAIS).

0 = transmit data normally
 1 = transmit an unframed all-ones code at TPOS and TNEG

Bit 0: Transmit CRC-4 Enable (TCRC4).

0 = CRC-4 disabled
 1 = CRC-4 enabled

Register Name: **TCR2 (T1 Mode)**
 Register Description: **Transmit Control Register 2**
 Register Address: **182h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|--------|---|-------|-------|-------|-----|-------|
| Name | TFDLS | TSLC96 | — | FBCT2 | FBCT1 | TD4RM | PDE | TB7ZS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: See [TCR2](#) for E1 mode.

Bit 7: TFDL Register Select (TFDLS).

- 0 = source FDL or Fs bits from the internal TFDL register or the SLC-96 data formatter (TCR2.6)
- 1 = source FDL or Fs bits from the internal HDLC controller

Bit 6: Transmit SLC-96 (TSLC96). Set this bit to a one in SLC-96 framing applications. Must be set to source the SLC-96 alignment pattern and data from the [T1TSLC1:T1TSLC3](#) registers. See Section [8.9.4.4](#) for details.

- 0 = SLC-96 insertion disabled
- 1 = SLC-96 insertion enabled

Bit 4: F-Bit Corruption Type 2 (FBCT2). Setting this bit high enables the corruption of one Ft (D4 framing mode) or FPS (ESF framing mode) bit in every 128 Ft or FPS bits as long as the bit remains set.

Bit 3: F-Bit Corruption Type 1 (FBCT1). A low-to-high transition of this bit causes the next three consecutive Ft (D4 framing mode) or FPS (ESF framing mode) bits to be corrupted causing the remote end to experience a loss of synchronization.

Bit 2: Transmit D4 RAI Select (TD4RM).

- 0 = zeros in bit 2 of all channels
- 1 = a one in the S-bit position of frame 12

Bit 1: Pulse Density Enforcer Enable (PDE). The framer always examines both the transmit and receive data streams for violations of the following rules which are required by ANSI T1.403: no more than 15 consecutive zeros and at least N ones in each and every time window of $8 \times (N + 1)$ bits where $N = 1$ through 23. Violations for the transmit and receive data streams are reported in the [TLS1.3](#) and [RLS2.7](#) bits, respectively. When this bit is set to one, the DS26524 will force the transmitted stream to meet this requirement no matter the content of the transmitted stream. When running B8ZS, this bit should be set to zero since B8ZS-encoded data streams cannot violate the pulse density requirements.

- 0 = disable transmit pulse density enforcer
- 1 = enable transmit pulse density enforcer

Bit 0: Transmit-Side Bit 7 Zero-Suppression Enable (TB7ZS).

- 0 = no stuffing occurs
- 1 = force bit 7 to a one as determined by the GB7S bit at [TCR1.3](#)

Register Name: **TCR2 (E1 Mode)**
 Register Description: **Transmit Control Register 2**
 Register Address: **182h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|-----|------|------|------|------|------|
| Name | AEBE | AAIS | ARA | Sa4S | Sa5S | Sa6S | Sa7S | Sa8S |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: See [TCR2](#) for T1 mode.

Bit 7: Automatic E-Bit Enable (AEBE).

- 0 = E-bits not automatically set in the transmit direction
- 1 = E-bits automatically set in the transmit direction

Bit 6: Automatic AIS Generation (AAIS).

- 0 = disabled
- 1 = enabled

Bit 5: Automatic Remote Alarm Generation (ARA).

- 0 = disabled
- 1 = enabled

Bit 4: Sa4 Bit Select (Sa4S). Set to one to source the Sa4 bit; set to zero to not source the Sa4 bit.

Bit 3: Sa5 Bit Select (Sa5S). Set to one to source the Sa5 bit; set to zero to not source the Sa5 bit.

Bit 2: Sa6 Bit Select (Sa6S). Set to one to source the Sa6 bit; set to zero to not source the Sa6 bit

Bit 1: Sa7 Bit Select (Sa7S). Set to one to source the Sa7 bit; set to zero to not source the Sa7 bit.

Bit 0: Sa8 Bit Select (Sa8S). Set to one to source the Sa8 bit; set to zero to not source the Sa8 bit.

Register Name: **TCR3**
 Register Description: **Transmit Control Register 3**
 Register Address: **183h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------------|------------|--------------|--------------|-------------|-----|-------------|--------------|
| Name | ODF | ODM | TCSS1 | TCSS0 | MFRS | TFM | IBPV | TLOOP |
| | <i>ODF</i> | <i>ODM</i> | <i>TCSS1</i> | <i>TCSS0</i> | <i>MFRS</i> | — | <i>IBPV</i> | <i>CRC4R</i> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Output Data Format (ODF).

0 = bipolar data at TTIP and TRING
 1 = NRZ data at TTIP; TRING = 0

Bit 6: Output Data Mode (ODM).

0 = pulses at TTIP and TRING are one full TCLK period wide
 1 = pulses at TTIP and TRING are 1/2 TCLK period wide

Bits 5 and 4: Transmit Clock Source Select 1 and 0 (TCSS[1:0]).

| TCSS1 | TCSS0 | TRANSMIT CLOCK SOURCE |
|-------|-------|---|
| 0 | 0 | The TCLK pin is always the source of transmit clock. |
| 0 | 1 | Switch to the clock present at RCLK when the signal at the TCLK pin fails to transition after one channel time. |
| 1 | 0 | Reserved |
| 1 | 1 | Use the signal present at RCLK as the transmit clock. The TCLK pin is ignored. |

Bit 3: Multiframe Reference Select (MFRS). This bit selects the source for the transmit formatter multiframe boundary.

0 = Normal operation. Transmit multiframe boundary is determined by line-side counters referenced to TSYNC when TSYNC is an input. Free-running when TSYNC is an output.

1 = Pass-forward operation. Transmit multiframe boundary determined by system-side counters referenced to TSSYNCIO (input mode 3), which is then passed forward to the line-side clock domain. This mode can only be used when the transmit elastic store is enabled with a synchronous backplane (i.e., no frame slips allowed). This mode must be used to allow transmit hardware-signaling insertion while the transmit elastic store is enabled.

Bit 2: Transmit Frame Mode Select (TFM) (T1 Mode Only).

0 = ESF framing mode
 1 = D4 framing mode

Bit 1: Insert BPV (IBPV). A 0-to-1 transition on this bit will cause a single bipolar violation (BPV) to be inserted into the transmit data stream. Once this bit has been toggled from 0 to 1, the device waits for the next occurrence of three consecutive ones to insert the BPV. This bit must be cleared and set again for a subsequent error to be inserted.

Bit 0 (T1 Mode): Transmit Loop Code Enable (TLOOP). See Section [8.9.15](#) for details.

0 = transmit data normally
 1 = replace normal transmitted data with repeating code as defined in registers [T1TCD1](#) and [T1TCD2](#)

Bit 0 (E1 Mode): CRC-4 Recalculate (CRC4R).

0 = transmit CRC-4 generation and insertion operates in normal mode
 1 = transmit CRC-4 generation operates according to G.706 Intermediate Path Recalculation method

Register Name: **TIOCR**
 Register Description: **Transmit I/O Configuration Register**
 Register Address: **184h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|----------|-----------|--------|------|------|------|-----|
| Name | TCLKINV | TSYNCINV | TSSYNCINV | TSCLKM | TSSM | TSIO | TSDW | TSM |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | — | TSM |

Bit 7: TCLK Invert (TCLKINV).

0 = No inversion
 1 = Invert

Bit 6: TSYNC Invert (TSYNCINV).

0 = No inversion
 1 = Invert

Bit 5: TSSYNCIO Invert (TSSYNCINV) (Input Mode Only).

0 = No inversion
 1 = Invert

Bit 4: TSYCLK Mode Select (TSCLKM).

0 = if TSYCLK is 1.544MHz
 1 = if TSYCLK is 2.048/4.096/8.192MHz or IBO enabled (see Section [8.8.2](#) for details on IBO function)

Bit 3: TSSYNCIO Mode Select (TSSM). Selects frame or multiframe mode for the TSSYNCIO pin.

0 = frame mode
 1 = multiframe mode

Bit 2: TSYNC I/O Select (TSIO).

0 = TSYNC is an input
 1 = TSYNC is an output

Bit 1: TSYNC Double-Wide (TSDW) (T1 Mode Only). (Note: This bit must be set to zero when TSM = 1 or when TSIO = 0.)

0 = do not pulse double-wide in signaling frames
 1 = do pulse double-wide in signaling frames

Bit 0: TSYNC Mode Select (TSM). Selects frame or multiframe mode for the TSYNC pin.

0 = frame mode
 1 = multiframe mode

Register Name: **TESCR**
 Register Description: **Transmit Elastic Store Control Register**
 Register Address: **185h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---|------|---------|------|--------|------|
| Name | TDATFMT | TGCLKEN | — | TSZS | TESALGN | TESR | TESMDM | TESE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: Bits 7 and 6 are used for fractional backplane support. See Section [8.8.5](#).

Bit 7: Transmit Channel Data Format (TDATFMT).

- 0 = 64kbps (data contained in all 8 bits)
- 1 = 56kbps (data contained in 7 out of the 8 bits)

Bit 6: Transmit Gapped-Clock Enable (TGCLKEN).

- 0 = TCHCLK functions normally
- 1 = enable gapped bit clock output on TCHCLK

Bit 4: Transmit Slip Zone Select (TSZS). This bit determines the minimum distance allowed between the elastic store read and write pointers before forcing a controlled slip. This bit is only applies during T1-to-E1 or E1-to-T1 conversion applications.

- 0 = force a slip at 9 bytes or less of separation (used for clustered blank channels)
- 1 = force a slip at 2 bytes or less of separation (used for distributed blank channels)

Bit 3: Transmit Elastic Store Align (TESALGN). Setting this bit from 0 to 1 will force the transmit elastic store's write/read pointers to a minimum separation of half a frame. No action will be taken if the pointer separation is already greater or equal to half a frame. If pointer separation is less than half a frame, the command will be executed and the data will be disrupted. Should be toggled after TSYCLK has been applied and is stable. Must be cleared and set again for a subsequent align.

Bit 2: Transmit Elastic Store Reset (TESR). Setting this bit from 0 to 1 will force the read pointer into the same frame that the write pointer is exiting, minimizing the delay through the elastic store. If this command should place the pointers within the slip zone (see bit 4), then an immediate slip will occur and the pointers will move back to opposite frames. Should be toggled after TSYCLK has been applied and is stable. Do not leave this bit set HIGH.

Bit 1: Transmit Elastic Store Minimum-Delay Mode (TESMDM).

- 0 = elastic stores operate at full two-frame depth
- 1 = elastic stores operate at 32-bit depth

Bit 0: Transmit Elastic Store Enable (TESE).

- 0 = elastic store is bypassed
- 1 = elastic store is enabled

Register Name: **TCR4 (T1 Mode Only)**
 Register Description: **Transmit Control Register 4**
 Register Address: **186h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|-------|-------|-----|-----|
| Name | — | — | — | — | TRAIM | TAISM | TC1 | TC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 3: Transmit RAI Mode (TRAIM). Determines the pattern sent when TRAI ([TCR1.0](#)) is activated in ESF frame mode only.

- 0 = transmit normal RAI upon activation with [TCR1.0](#)
- 1 = transmit RAI-CI (T1.403) upon activation with [TCR1.0](#)

Bits 2: Transmit AIS Mode (TAISM). Determines the pattern sent when TAIS ([TCR1.1](#)) is activated.

- 0 = transmit normal AIS (unframed all ones) upon activation with [TCR1.1](#)
- 1 = transmit AIS-CI (T1.403) upon activation with [TCR1.1](#)

Bits 1 and 0: Transmit Code Length Definition Bits (TC[1:0]).

| TC1 | TC0 | LENGTH SELECTED (BITS) |
|-----|-----|------------------------|
| 0 | 0 | 5 |
| 0 | 1 | 6 : 3 |
| 1 | 0 | 7 |
| 1 | 1 | 16 : 8 : 4 : 2 : 1 |

Register Name: **THFC**
 Register Description: **Transmit HDLC FIFO Control Register**
 Register Address: **187h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|--------|--------|
| Name | — | — | — | — | — | — | TFLWM1 | TFLWM2 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 1 and 0: Transmit HDLC FIFO Low Watermark Select (TFLWM[1:2]).

| TFLWM1 | TFLWM2 | TRANSMIT FIFO WATERMARK (BYTES) |
|--------|--------|---------------------------------|
| 0 | 0 | 4 |
| 0 | 1 | 16 |
| 1 | 0 | 32 |
| 1 | 1 | 48 |

Register Name: **TIBOC**
 Register Description: **Transmit Interleave Bus Operation Control Register**
 Register Address: **188h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|------|------|--------|-------|-----|-----|-----|
| Name | — | IBS1 | IBS0 | IBOSEL | IBOEN | DA2 | DA1 | DA0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 6 and 5: IBO Bus Size (IBS[1:0]). Indicates how many devices are on the bus.

| IBS1 | IBS0 | BUS SIZE |
|------|------|-------------------------|
| 0 | 0 | 2 devices on bus |
| 0 | 1 | 4 devices on bus |
| 1 | 0 | 8 devices on bus |
| 1 | 1 | Reserved for future use |

Bit 4: Interleave Bus Operation Select (IBOSEL). This bit selects channel or frame interleave mode.
 0 = Channel Interleave
 1 = Frame Interleave

Bit 3: Interleave Bus Operation Enable (IBOEN).
 0 = Interleave Bus Operation disabled
 1 = Interleave Bus Operation enabled

Bits 2 to 0: Device Assignment Bits (DA[2:0]).

| DA2 | DA1 | DA0 | DEVICE POSITION |
|-----|-----|-----|-------------------|
| 0 | 0 | 0 | 1st device on bus |
| 0 | 0 | 1 | 2nd device on bus |
| 0 | 1 | 0 | 3rd device on bus |
| 0 | 1 | 1 | 4th device on bus |
| 1 | 0 | 0 | 5th device on bus |
| 1 | 0 | 1 | 6th device on bus |
| 1 | 1 | 0 | 7th device on bus |
| 1 | 1 | 1 | 8th device on bus |

Register Name: **TDS0SEL**
 Register Description: **Transmit DS0 Channel Monitor Select Register**
 Register Address: **189h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|------|------|------|------|------|
| Name | — | — | — | TCM4 | TCM3 | TCM2 | TCM1 | TCM0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 4 to 0: Transmit Channel Monitor Bits (TCM[4:0]). TCM0 is the LSB of a 5-bit channel select that determines which transmit channel data will appear in the [TDS0M](#) register. Channels 1 to 32 are represented by a 5-bit BCD code from 0 to 31. TCM[4:0] = all zeros selects channel 1, TCM[4:0] = 11111 selects channel 32.

Register Name: **TXPC**
 Register Description: **Transmit Expansion Port Control Register**
 Register Address: **18Ah + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|--------|--------|-------|
| Name | — | — | — | — | — | TBPDIR | TBPFUS | TBPEN |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 2: Transmit BERT Port Direction Control (TBPDIR).

0 = Normal (line) operation. Transmit BERT port sources data into the transmit path.

1 = System (backplane) operation. Transmit BERT port sources data into the receive path (RDATA). In this mode the data out of the transmit BERT is muxed into the receive path at RDATA (the line side of the elastic store).

Bit 1: Transmit BERT Port Framed/Unframed Select (TBPFUS).

0 = The transmit BERT will *not* clock data into the F-bit position (framed)

1 = The transmit BERT will clock data into the F-bit position (unframed)

Bit 0: Transmit BERT Port Enable (TBPEN).

0 = Transmit BERT port is not active

1 = Transmit BERT port is active

Register Name: **TBPBS**
 Register Description: **Transmit BERT Port Bit Suppress Register**
 Register Address: **18Bh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Name | BPBSE8 | BPBSE7 | BPBSE6 | BPBSE5 | BPBSE4 | BPBSE3 | BPBSE2 | BPBSE1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit Channel Bit 8 Suppress (BPBSE8). MSB of the channel. Set to one to stop this bit from being used.

Bit 6: Transmit Channel Bit 7 Suppress (BPBSE7). Set to one to stop this bit from being used.

Bit 5: Transmit Channel Bit 6 Suppress (BPBSE6). Set to one to stop this bit from being used.

Bit 4: Transmit Channel Bit 5 Suppress (BPBSE5). Set to one to stop this bit from being used.

Bit 3: Transmit Channel Bit 4 Suppress (BPBSE4). Set to one to stop this bit from being used.

Bit 2: Transmit Channel Bit 3 Suppress (BPBSE3). Set to one to stop this bit from being used.

Bit 1: Transmit Channel Bit 2 Suppress (BPBSE2). Set to one to stop this bit from being used.

Bit 0: Transmit Channel Bit 1 Suppress (BPBSE1). LSB of the channel. Set to one to stop this bit from being used.

Register Name: **TSYNCC**
 Register Description: **Transmit Synchronizer Control Register**
 Register Address: **18Eh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|------|------|-------|--------|
| Name | — | — | — | — | — | TSEN | SYNCE | RESYNC |
| | — | — | — | — | CRC4 | TSEN | SYNCE | RESYNC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 3: CRC-4 Enable (CRC4) (E1 Mode Only).

0 = Do not search for the CRC-4 multiframe word

1 = Search for the CRC-4 multiframe word

Bit 2: Transmit Synchronizer Enable (TSEN).

0 = Transmit synchronizer disabled

1 = Transmit synchronizer enabled

Bit 1: Sync Enable (SYNCE).

0 = auto resync enabled

1 = auto resync disabled

Bit 0: Resynchronize (RESYNC). When toggled from low to high, a resynchronization of the transmit-side framer is initiated. Must be cleared and set again for a subsequent resync.

Register Name: **TLS1**
 Register Description: **Transmit Latched Status Register 1**
 Register Address: **190h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|--------------|--------------|--------|------------|------------|--------------|--------------|
| Name | TESF | TESEM | TSLIP | TSLC96 | TPDV | TMF | LOTCC | LOTCC |
| | <i>TESF</i> | <i>TESEM</i> | <i>TSLIP</i> | — | <i>TAF</i> | <i>TMF</i> | <i>LOTCC</i> | <i>LOTCC</i> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are latched and can cause interrupts.

Bit 7: Transmit Elastic Store Full Event (TESF). Set when the transmit elastic store buffer fills and a frame is deleted.

Bit 6: Transmit Elastic Store Empty Event (TESEM). Set when the transmit elastic store buffer empties and a frame is repeated.

Bit 5: Transmit Elastic Store Slip Occurrence Event (TSLIP). Set when the transmit elastic store has either repeated or deleted a frame.

Bit 4: Transmit SLC-96 Multiframe Event (TSLC96) (T1 Mode Only). When enabled by [TCR2.6](#), this bit will set once per SLC-96 multiframe (72 frames) to alert the host that new data may be written to the [T1TSLC1:T1TSLC3](#) registers. See Section [8.9.4.4](#) for more information.

Bit 3 (T1 Mode): Transmit Pulse Density Violation Event (TPDV). Set when the transmit data stream does not meet the ANSI T1.403 requirements for pulse density.

Bit 3 (E1 Mode): Transmit Align Frame Event (TAF). Set every 250µs to alert the host that the [E1TAF](#) and [E1TNAF](#) registers need to be updated.

Bit 2: Transmit Multiframe Event (TMF). In T1 mode, this bit is set every 1.5ms on D4 MF boundaries or every 3ms on ESF MF boundaries. In E1 operation, this bit is set every 2ms (regardless if CRC-4 is enabled) on transmit multiframe boundaries. Used to alert the host that signaling data needs to be updated.

Bit 1: Loss of Transmit Clock Condition Clear (LOTCC). Set when the LOTC condition has cleared (a clock has been sensed at the TCLK pin).

Bit 0: Loss of Transmit Clock Condition (LOTCC). Set when the TCLK pin has not transitioned for approximately 3 clock periods. Will force the LOTC bit high if enabled. This bit can be cleared by the host even if the condition is still present. LOTC will remain high while the condition exists, even if the host has cleared the status bit. If enabled by [TIM1.0](#), the $\overline{\text{INTB}}$ pin will transition low when this bit is set, and transition high when this bit is cleared (if no other unmasked interrupt conditions exist).

Register Name: **TLS2**
 Register Description: **Transmit Latched Status Register 2 (HDLC)**
 Register Address: **191h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|-------|------|-------|-------|------|
| Name | — | — | — | TFDLE | TUDR | TMEND | TLWMS | TNFS |
| | — | — | — | — | TUDR | TMEND | TLWMS | TNFS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are latched and can create interrupts.

Bit 4: Transmit FDL Register Empty (TFDLE) (T1 Mode Only). Set when the TFDL register has shifted out all 8 bits. Useful if the user wants to manually use the TFDL register to send messages, instead of using the HDLC or BOC controller circuits.

Bit 3: Transmit FIFO Underrun Event (TUDR). Set when the transmit FIFO empties out without having seen the TMEND bit set. An abort is automatically sent.

Bit 2: Transmit Message End Event (TMEND). Set when the transmit HDLC controller has finished sending a message.

Bit 1: Transmit FIFO Below Low Watermark Set Condition (TLWMS). Set when the transmit 64-byte FIFO empties beyond the low watermark as defined by the transmit low watermark bit (TLWM), rising edge detect of TLWM.

Bit 0: Transmit FIFO Not Full Set Condition (TNFS). Set when the transmit 64-byte FIFO has at least one empty byte available for write. Rising edge detect of TNF. Indicates change of state from full to not full.

Register Name: **TLS3**
 Register Description: **Transmit Latched Status Register 3 (Synchronizer)**
 Register Address: **192h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|-----|------|
| Name | — | — | — | — | — | — | LOF | LOFD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: Some bits in this register are latched and can create interrupts.

Bit 1: Loss of Frame (LOF). A real-time bit that indicates that the transmit synchronizer is searching for the sync pattern in the incoming data stream.

Bit 0: Loss of Frame Synchronization Detect (LOFD). This latched bit is set when the transmit synchronizer is searching for the sync pattern in the incoming data stream.

Register Name: **TIIR**
 Register Description: **Transmit Interrupt Information Register**
 Register Address: **19Fh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|------|------|------|
| Name | — | — | — | — | — | TLS3 | TLS2 | TLS1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The Transmit Interrupt Information register provides an indication of which status registers are generating an interrupt. When an interrupt occurs, the host can read TIIR to quickly identify which of the transmit status registers are causing the interrupt(s). These are real-time registers in that the bits will clear once the appropriate interrupt has been serviced and cleared.

Bit 2: Transmit Latched Status Register 3 Interrupt Status (TLS3).

0 = no interrupt pending
 1 = interrupt pending

Bit 1: Transmit Latched Status Register 2 Interrupt Status (TLS2).

0 = no interrupt pending
 1 = interrupt pending

Bit 0: Transmit Latched Status Register 1 Interrupt Status (TLS1).

0 = no interrupt pending
 1 = interrupt pending

Register Name: **TIM1**
 Register Description: **Transmit Interrupt Mask Register 1**
 Register Address: **1A0h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|--------------|--------------|--------|------------|------------|--------------|--------------|
| Name | TESF | TESEM | TSLIP | TSLC96 | TPDV | TMF | LOTCC | LOTCC |
| | <i>TESF</i> | <i>TESEM</i> | <i>TSLIP</i> | — | <i>TAF</i> | <i>TMF</i> | <i>LOTCC</i> | <i>LOTCC</i> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit Elastic Store Full Event (TESF).

0 = interrupt masked
 1 = interrupt enabled

Bit 6: Transmit Elastic Store Empty Event (TESEM).

0 = interrupt masked
 1 = interrupt enabled

Bit 5: Transmit Elastic Store Slip Occurrence Event (TSLIP).

0 = interrupt masked
 1 = interrupt enabled

Bit 4: Transmit SLC-96 Multiframe Event (TSLC96) (T1 Mode Only).

0 = interrupt masked
 1 = interrupt enabled

Bit 3 (T1 Mode): Transmit Pulse Density Violation Event (TPDV).

0 = interrupt masked
 1 = interrupt enabled

Bit 3 (E1 Mode): Transmit Align Frame Event (TAF).

0 = interrupt masked
 1 = interrupt enabled

Bit 2: Transmit Multiframe Event (TMF).

0 = interrupt masked
 1 = interrupt enabled

Bit 1: Loss of Transmit Clock Clear Condition (LOTCC).

0 = interrupt masked
 1 = interrupt enabled

Bit 0: Loss of Transmit Clock Condition (LOTCC).

0 = interrupt masked
 1 = interrupt enabled

Register Name: **TIM2**
 Register Description: **Transmit Interrupt Mask Register 2 (HDLC)**
 Register Address: **1A1h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|-------|------|-------|-------|------|
| Name | — | — | — | TFDLE | TUDR | TMEND | TLWMS | TNFS |
| | — | — | — | — | TUDR | TMEND | TLWMS | TNFS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 4: Transmit FDL Register Empty (TFDLE) (T1 Mode Only).

0 = interrupt masked
 1 = interrupt enabled

Bit 3: Transmit FIFO Underrun Event (TUDR).

0 = interrupt masked
 1 = interrupt enabled

Bit 2: Transmit Message End Event (TMEND).

0 = interrupt masked
 1 = interrupt enabled

Bit 1: Transmit FIFO Below Low Watermark Set Condition (TLWMS).

0 = interrupt masked
 1 = interrupt enabled

Bit 0: Transmit FIFO Not Full Set Condition (TNFS).

0 = interrupt masked
 1 = interrupt enabled

Register Name: **TIM3**
 Register Description: **Transmit Interrupt Mask Register 3 (Synchronizer)**
 Register Address: **1A2h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|------|
| Name | — | — | — | — | — | — | — | LOFD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Loss of Frame Synchronization Detect (LOFD).

0 = interrupt masked
 1 = interrupt enabled

Register Name: **T1TCD1 (T1 Mode Only)**
 Register Description: **Transmit Code Definition Register 1**
 Register Address: **1ACh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit Code Definition Bit 7 (C7). First bit of the repeating pattern.

Bit 6: Transmit Code Definition Bit 6 (C6).

Bit 5: Transmit Code Definition Bit 5 (C5).

Bit 4: Transmit Code Definition Bit 4 (C4).

Bit 3: Transmit Code Definition Bit 3 (C3).

Bit 2: Transmit Code Definition Bit 2 (C2). A Don't Care if a 5-bit length is selected.

Bit 1: Transmit Code Definition Bit 1 (C1). A Don't Care if a 5- or 6-bit length is selected.

Bit 0: Transmit Code Definition Bit 0 (C0). A Don't Care if a 5-, 6-, or 7-bit length is selected.

Register Name: **T1TCD2 (T1 Mode Only)**
 Register Description: **Transmit Code Definition Register 2**
 Register Address: **1ADh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit Code Definition Bit 7 (C7). A Don't Care if a 5-, 6-, or 7-bit length is selected.

Bit 6: Transmit Code Definition Bit 6 (C6). A Don't Care if a 5-, 6-, or 7-bit length is selected.

Bit 5: Transmit Code Definition Bit 5 (C5). A Don't Care if a 5-, 6-, or 7-bit length is selected.

Bit 4: Transmit Code Definition Bit 4 (C4). A Don't Care if a 5-, 6-, or 7-bit length is selected.

Bit 3: Transmit Code Definition Bit 3 (C3). A Don't Care if a 5-, 6-, or 7-bit length is selected.

Bit 2: Transmit Code Definition Bit 2 (C2). A Don't Care if a 5-, 6-, or 7-bit length is selected.

Bit 1: Transmit Code Definition Bit 1 (C1). A Don't Care if a 5-, 6-, or 7-bit length is selected.

Bit 0: Transmit Code Definition Bit 0 (C0). A Don't Care if a 5-, 6-, or 7-bit length is selected.

Register Name: **TRTS2**
 Register Description: **Transmit Real-Time Status Register 2 (HDLC)**
 Register Address: **1B1h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|-------|-------|------|-----|
| Name | — | — | — | — | EMPTY | TFULL | TLWM | TNF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are real time.

Bit 3: Transmit FIFO Empty (EMPTY). A real-time bit that is set high when the FIFO is empty.

Bit 2: Transmit FIFO Full (TFULL). A real-time bit that is set high when the FIFO is full.

Bit 1: Transmit FIFO Below Low Watermark Condition (TLWM). Set when the transmit 64-byte FIFO empties beyond the low watermark as defined by the transmit low watermark bits (TLWM).

Bit 0: Transmit FIFO Not Full Condition (TNF). Set when the transmit 64-byte FIFO has at least one byte available.

Register Name: **TFBA**
 Register Description: **Transmit HDLC FIFO Buffer Available**
 Register Address: **1B3h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|-------|-------|-------|-------|-------|-------|-------|
| Name | — | TFBA6 | TFBA5 | TFBA4 | TFBA3 | TFBA2 | TFBA1 | TFBA0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 6 to 0: Transmit FIFO Bytes Available (TFBA[6:0]). TFBA0 is the LSB.

Register Name: **THF**
 Register Description: **Transmit HDLC FIFO Register**
 Register Address: **1B4h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | THD7 | THD6 | THD5 | THD4 | THD3 | THD2 | THD1 | THD0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit HDLC Data Bit 7 (THD7). MSB of an HDLC packet data byte.

Bit 6: Transmit HDLC Data Bit 6 (THD6).

Bit 5: Transmit HDLC Data Bit 5 (THD5).

Bit 4: Transmit HDLC Data Bit 4 (THD4).

Bit 3: Transmit HDLC Data Bit 3 (THD3).

Bit 2: Transmit HDLC Data Bit 2 (THD2).

Bit 1: Transmit HDLC Data Bit 1 (THD1).

Bit 0: Transmit HDLC Data Bit 0 (THD0). LSB of an HDLC packet data byte.

Register Name: **TDS0M**
 Register Description: **Transmit DS0 Monitor Register**
 Register Address: **1BBh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Transmit DS0 Channel Bits (B[1:8]). Transmit channel data that has been selected by the Transmit DS0 Channel Monitor Select register ([TDS0SEL](#)). B8 is the LSB of the DS0 channel (last bit to be transmitted).

Register Name: **TBCS1, TBCS2, TBCS3, TBCS4**
 Register Description: **Transmit Blank Channel Select Registers 1 to 4**
 Register Address: **1C0h, 1C1h, 1C2h, 1C3h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | (MSB) 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) | |
|---------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|---------------------------------------|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | TBCS1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | TBCS2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | TBCS3 |
| | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> | TBCS4 (E1 Mode Only) |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Bits 7 to 0: Transmit Blank Channel Select for Channels 1 to 32 (CH[1:32]).

0 = transmit TSER data from this channel

1 = ignore TSER data from this channel

Note that when two or more sequential channels are chosen to be ignored, the receive slip zone select bit should be set to zero. If the ignore channels are distributed (such as 1, 5, 9, 13, 17, 21, 25, 29), the RSZS bit can be set to one, which may provide a lower occurrence of slips in certain applications.

Register Name: **TCBR1, TCBR2, TCBR3, TCBR4**
 Register Description: **Transmit Channel Blocking Registers 1 to 4**
 Register Address: **1C4h, 1C5h, 1C6h, 1C7h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | (MSB) | | | | | | | (LSB) | |
|---------|-------|------|------|------|------|------|------|-----------------|--------------------------|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | TCBR1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | TCBR2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | TCBR3 |
| | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 (F-bit) | TCBR4* (E1 Mode Only) |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Bits 7 to 0: Transmit Channel Blocking Channels 1 to 32 Control Bits (CH[1:32]).

0 = force the TCHBLK pin to remain low during this channel time

1 = force the TCHBLK pin high during this channel time

***Note that TCBR4 has two functions:**

When 2.048MHz backplane mode is selected, this register allows the user to enable the channel blocking signal for any of the 32 possible backplane channels.

When 1.544MHz backplane mode is selected, the LSB of this register determines whether or not the TCHBLK signal will pulse high during the F-bit time:

TCBR4.0 = 0: Do not pulse TCHBLK during the F-bit.

TCBR4.0 = 1: Pulse TCHBLK during the F-bit.

In this mode, TCBR4.1 to TCBR4.7 should be set to 0.

Register Name: **THSCS1, THSCS2, THSCS3, THSCS4**
 Register Description: **Transmit Hardware-Signaling Channel Select Registers 1 to 4**
 Register Address: **1C8h, 1C9h, 1CAh, 1CBh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | (MSB) 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) | |
|---------|---------|------|------|------|------|------|------|---------|---------------------------|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | THSCS1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | THSCS2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | THSCS3 |
| | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | THSCS4* (E1 Mode Only) |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Bits 7 to 0: Transmit Hardware-Signaling Channel Select for Channels 1 to 32 (CH[1:32]). These bits determine which channels have signaling data inserted from the TSIG pin into the TSER PCM data.

0 = do not source signaling data from the TSIG pin for this channel

1 = source signaling data from the TSIG pin for this channel

***Note that THSCS4 is only used in 2.048MHz backplane applications.**

Register Name: **TGCCS1, TGCCS2, TGCCS3, TGCCS4**
 Register Description: **Transmit Gapped-Clock Channel Select Registers 1 to 4**
 Register Address: **1CCh, 1CDh, 1CEh, 1CFh + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | (MSB) | | | | | | | (LSB) | |
|---------|-------|------|------|------|------|------|------|-----------------|---------------------------|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | TGCCS1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | TGCCS2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | TGCCS3 |
| | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 (F-bit) | TGCCS4* (E1 Mode Only) |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Bits 7 to 0: Transmit Gapped-Clock Channel Select Channels 1 to 32 (CH[1:32]).

0 = no clock is present on TCHCLK during this channel time

1 = force a clock on TCHCLK during this channel time. The clock will be synchronous with TCLK if the elastic store is disabled, and synchronous with TSYCLK if the elastic store is enabled.

***Note that TGCCS4 has two functions:**

When 2.048MHz backplane mode is selected, this register allows the user to enable the gapped clock on TCHCLK for any of the 32 possible backplane channels.

When 1.544MHz backplane mode is selected, the LSB of this register determines whether or not a clock is generated on TCHCLK during the F-bit time:

TGCCS4.0 = 0: Do not generate a clock during the F-bit

TGCCS4.0 = 1: Generate a clock during the F-bit

In this mode, TGCCS4.1 to TGCCS4.7 should be set to 0.

Register Name: **PCL1, PCL2, PCL3, PCL4**
 Register Description: **Per-Channel Loopback Enable Registers 1 to 4**
 Register Address: **1D0h, 1D1h, 1D2h, 1D3h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | (MSB) | | | | | | | (LSB) | |
|---------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|--------------------------------|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | PCL1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | PCL2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | PCL3 |
| | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> | PCL4 (E1 Mode Only) |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Bits 7 to 0: Per-Channel Loopback Enable for Channels 1 to 32 (CH[1:32]).

0 = loopback disabled

1 = enable loopback; source data from the corresponding receive channel

Register Name: **TBPCS1, TBPCS2, TBPCS3, TBPCS4**
 Register Description: **Transmit BERT Port Channel Select Registers 1 to 4**
 Register Address: **1D4h, 1D5h, 1D6h, 1D7h + (200h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | (MSB) 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) | |
|---------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|----------------------------------|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | TBPCS1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | TBPCS2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | TBPCS3 |
| | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> | TBPCS4 (E1 Mode Only) |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Setting any of the CH[1:32] bits in the TBPCS1:TBPCS4 registers will enable the transmit BERT clock for the associated channel time, and allow mapping of the selected channel data out of the receive BERT port. Multiple or all channels can be selected simultaneously.

9.5 LIU Register Definitions

Table 9-14. LIU Register Set

| ADDRESS | NAME | DESCRIPTION | R/W |
|-------------|------------------------|---|-----|
| 1000h | LTRCR | LIU Transmit Receive Control Register | R/W |
| 1001h | LTITSR | LIU Transmit Impedance and Pulse Shape Selection Register | R/W |
| 1002h | LMCR | LIU Maintenance Control Register | R/W |
| 1003h | LRSR | LIU Real Status Register | R |
| 1004h | LSIMR | LIU Status Interrupt Mask Register | R/W |
| 1005h | LLSR | LIU Latched Status Register | R/W |
| 1006h | LRSL | LIU Receive Signal Level Register | R |
| 1007h | LRISMR | LIU Receive Impedance and Sensitivity Monitor Register | R/W |
| 1008h–101Fh | — | Reserved | — |

Note: Reserved registers should only be written with all zeros.

Register Name: **LTRCR**
 Register Description: **LIU Transmit Receive Control Register**
 Register Address: **1000h + (20h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|------|-------|-------|---------|-----|
| Name | — | — | — | JADS | JAPS1 | JAPS0 | T1J1E1S | LSC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 4: Jitter Attenuator Depth Select (JADS).

0 = Jitter attenuator FIFO depth set to 128 bits.

1 = Jitter attenuator FIFO depth set to 32 bits. Use for delay-sensitive applications.

Bits 3 and 2: Jitter Attenuator Position Select 1 and 0 (JAPS[1:0]). These bits are used to select the position of the jitter attenuator.

| JAPS1 | JAPS0 | FUNCTION |
|-------|-------|--|
| 0 | 0 | Jitter attenuator is in the receive path. |
| 0 | 1 | Jitter attenuator is in the transmit path. |
| 1 | 0 | Jitter attenuator is not used. |
| 1 | 1 | Jitter attenuator is not used. |

Bit 1: T1J1E1 Selection (T1J1E1S). This bit configures the LIU for E1 or T1/J1 operation.

0 = E1

1 = T1 or J1

Bit 0: LOS Criteria Selection (LCS). This bit is used for LIU LOS selection criteria.

E1 Mode:

0 = G.775

1 = ETS 300 233

T1/J1 Mode:

0 = T1.231

1 = T1.231

Register Name: **LTITSR**
 Register Description: **LIU Transmit Impedance and Pulse Shape Selection Register**
 Register Address: **1001h + (20h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|----------|--------|--------|---|----|----|----|
| Name | — | TIMPTOFF | TIMPL1 | TIMPL0 | — | L2 | L1 | L0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 6: Transmit Impedance Off (TIMPTOFF).

0 = Enable transmit terminating impedance.
 1 = Disable transmit terminating impedance.

Bits 5 and 4: Transmit Load Impedance 1 and 0 (TIMPL[1:0]). These bits are used to select the transmit load impedance. These must be set to match the cable impedance. Even if the internal load impedance is turned off (via TIMPTOFF); the external cable impedance must be specified for optimum operation. For J1 applications, use 110Ω. See [Table 9-15](#).

Bits 2 to 0: Line Build-Out Select 2 to 0 (L[2:0]). Used to select the transmit waveshape. The waveshape has a voltage level and load impedance associated with it once the T1/J1 or E1 selection is made by settings in the [LTRCR](#) register. See [Table 9-16](#).

Table 9-15. Transmit Load Impedance Selection

| TIMPL1 | TIMPL0 | IMPEDANCE SELECTION |
|--------|--------|---------------------|
| 0 | 0 | 75Ω |
| 0 | 1 | 100Ω |
| 1 | 0 | 110Ω |
| 1 | 1 | 120Ω |

Table 9-16. Transmit Pulse Shape Selection

| L2 | L1 | L0 | MODE | IMPEDANCE | NOMINAL VOLTAGE |
|----|----|----|------|-----------|-----------------|
| 0 | 0 | 0 | E1 | 75Ω | 2.37V |
| 0 | 0 | 1 | E1 | 120Ω | 3.0V |

| L2 | L1 | L0 | MODE | CABLE LENGTH | MAX ALLOWED CABLE LOSS |
|----|----|----|-------|------------------------------------|------------------------|
| 0 | 0 | 0 | T1/J1 | DSX-1/0dB CSU, 0ft–133ft ABAM 100Ω | 0.6dB |
| 0 | 0 | 1 | T1/J1 | DSX-1, 133ft–266ft ABAM 100Ω | 1.2dB |
| 0 | 1 | 0 | T1/J1 | DSX-1, 266ft–399ft ABAM 100Ω | 1.8dB |
| 0 | 1 | 1 | T1/J1 | DSX-1, 399ft–533ft ABAM 100Ω | 2.4dB |
| 1 | 0 | 0 | T1/J1 | DSX-1, 533ft–655ft ABAM 100Ω | 3.0dB |
| 1 | 0 | 1 | T1/J1 | -7.5dB CSU | — |
| 1 | 1 | 0 | T1/J1 | -15dB CSU | — |
| 1 | 1 | 1 | T1/J1 | -22.5dB CSU | — |

Register Name: **LMCR**
 Register Description: **LIU Maintenance Control Register**
 Register Address: **1002h + (20h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|-------|-----|-----|-----|------|------|----|
| Name | TAIS | ATAIS | LLB | ALB | RLB | TPDE | RPDE | TE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit AIS (TAIS). Alarm Indication Signal (AIS) is sent using MCLK as the reference clock. The transmit data coming from the framer is ignored.

0 = TAIS is disabled.

1 = Output an unframed all-ones pattern (AIS) at TTIP and TRING.

Bit 6: Automatic Transmit AIS (ATAIS).

0 = ATAIS is disabled.

1 = Automatically transmit AIS on the occurrence of an LIU LOS.

Bit 5: Local Loopback (LLB). See Section [8.11.5.2](#) for operational details.

0 = LLB is disabled.

1 = LLB is enabled.

Bit 4: Analog Loopback (ALB). See Section [8.11.5.1](#) for operational details.

0 = ALB is disabled.

1 = ALB is enabled.

Bit 3: Remote Loopback (RLB). See Section [8.11.5.3](#) for operational details.

0 = Remote loopback is disabled.

1 = Remote loopback is enabled.

In this loopback, received data passes all the way through the receive LIU and is then transmitted back through the transmit side of the LIU. Data will continue to pass through the receive-side framer of the DS26524 as it would normally and the data from the transmit side of the framer will be ignored.

Bit 2: Transmit Power-Down Enable (TPDE).

0 = Transmitter power enabled.

1 = Transmitter powered down. TTIP/TRING outputs are high impedance.

Bit 1: Receiver Power-Down Enable (RPDE).

0 = Receiver power enabled.

1 = Receiver powered down.

Bit 0: Transmit Enable (TE). This function is overridden by the TXENABLE pin.

0 = TTIP/TRING outputs are high impedance.

1 = TTIP/TRING outputs enabled.

Register Name: **LRSR**
 Register Description: **LIU Real Status Register**
 Register Address: **1003h + (20h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|-----|-----|---|-----|-----|------|
| Name | — | — | OEQ | UEQ | — | SCS | OCS | LOSS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 5: Over Equalized (OEQ). The equalizer is over equalized. This can happen if there is very large unexpected resistive loss. This could result if monitor mode is used and the device is not placed in monitor mode. This indicator provides more qualitative information to the receive loss indicators.

Bit 4: Under Equalized (UEQ). The equalizer is under equalized. A signal with a very high resistive gain is being applied. This indicator provides more qualitative information to the receive loss indicators.

Bit 2: Short-Circuit Status (SCS). A real-time bit that is set when the LIU detects that the TTIP and TRING outputs are short-circuited. The load resistance must be 25Ω (typically) or less for short-circuit detection.

Bit 1: Open-Circuit Status (OCS). A real-time bit that is set when the LIU detects that the TTIP and TRING outputs are open-circuited.

Bit 0: Loss-of-Signal Status (LOSS). A real-time bit that is set when the LIU detects a LOS condition at RTIP and RRING.

Register Name: **LSIMR**
 Register Description: **LIU Status Interrupt Mask Register**
 Register Address: **1004h + (20h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|-------|-------|--------|---------|-------|-------|--------|
| Name | JALTCIM | OCCIM | SCCIM | LOSCIM | JALTSIM | OCDIM | SCDIM | LOSDIM |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Jitter Attenuator Limit Trip Clear Interrupt Mask (JALTCIM).

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 6: Open-Circuit Clear Interrupt Mask (OCCIM).

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 5: Short-Circuit Clear Interrupt Mask (SCCIM).

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 4: Loss of Signal Clear Interrupt Mask (LOSCIM).

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 3: Jitter Attenuator Limit Trip Set Interrupt Mask (JALTSIM).

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 2: Open-Circuit Detect Interrupt Mask (OCDIM).

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 1: Short-Circuit Detect Interrupt Mask (SCDIM).

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 0: Loss of Signal Detect Interrupt Mask (LOSDIM).

0 = Interrupt masked.
 1 = Interrupt enabled.

Register Name: **LLSR**
 Register Description: **LIU Latched Status Register**
 Register Address: **1005h + (20h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-----|-----|------|-------|-----|-----|------|
| Name | JALTC | OCC | SCC | LOSC | JALTS | OCD | SCD | LOSD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are latched and can create interrupts.

Bit 7: Jitter Attenuator Limit Trip Clear (JALTC). This latched bit is set when a jitter attenuator limit trip condition was detected and then removed.

Bit 6: Open-Circuit Clear (OCC). This latched bit is set when an open-circuit condition was detected at TTIP and TRING and then removed.

Bit 5: Short-Circuit Clear (SCC). This latched bit is set when a short-circuit condition was detected at TTIP and TRING and then removed.

Bit 4: Loss of Signal Clear (LOSC). This latched bit is set when a loss-of-signal condition was detected at RTIP and RRING and then removed.

Bit 3: Jitter Attenuator Limit Trip Set (JALTS). This latched bit is set when the jitter attenuator limit trip condition is detected.

Bit 2: Open-Circuit Detect (OCD). This latched bit is set when an open-circuit condition is detected at TTIP and TRING. This bit is not functional in T1 CSU operating modes (T1 LBO 5, LBO 6, and LBO 7).

Bit 1: Short-Circuit Detect (SCD). This latched bit is set when a short-circuit condition is detected at TTIP and TRING. This bit is not functional in T1 CSU operating modes (T1 LBO 5, LBO 6, and LBO 7).

Bit 0: Loss of Signal Detect (LOSD). This latched bit is set when an LOS condition is detected at RTIP and RRING.

Register Name: **LRSL**
 Register Description: **LIU Receive Signal Level Register**
 Register Address: **1006h + (20h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|---|---|---|---|
| Name | RSL3 | RSL2 | RLS1 | RLS0 | — | — | — | — |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 4: Receiver Signal Level 3 to 0 (RSL[3:0]). Real-time receive signal level as shown in [Table 9-17](#). Note that the range of signal levels reported the RSL[3:0] is limited by the Equalizer Gain Limit (EGL) in short-haul applications.

Table 9-17. Receive Level Indication

| RSL3 | RSL2 | RSL1 | RSL0 | RECEIVE LEVEL (dB) | |
|------|------|------|------|--------------------|--------------|
| | | | | T1 | E1 |
| 0 | 0 | 0 | 0 | > -2.5 | > -2.5 |
| 0 | 0 | 0 | 1 | -2.5 to -5 | -2.5 to -5 |
| 0 | 0 | 1 | 0 | -5 to -7.5 | -5 to -7.5 |
| 0 | 0 | 1 | 1 | -7.5 to -10 | -7.5 to -10 |
| 0 | 1 | 0 | 0 | -10 to -12.5 | -10 to -12.5 |
| 0 | 1 | 0 | 1 | -12.5 to -15 | -12.5 to -15 |
| 0 | 1 | 1 | 0 | -15 to -17.5 | -15 to -17.5 |
| 0 | 1 | 1 | 1 | -17.5 to -20 | -17.5 to -20 |
| 1 | 0 | 0 | 0 | -20 to -23 | -20 to -23 |
| 1 | 0 | 0 | 1 | -23 to -26 | -23 to -26 |
| 1 | 0 | 1 | 0 | -26 to -29 | -26 to -29 |
| 1 | 0 | 1 | 1 | -29 to -32 | -29 to -32 |
| 1 | 1 | 0 | 0 | -32 to -36 | -32 to -36 |
| 1 | 1 | 0 | 1 | < -36 | -36 to -40 |
| 1 | 1 | 1 | 0 | — | -40 to -44 |
| 1 | 1 | 1 | 1 | — | < -44 |

Register Name: **LRISMR**
 Register Description: **LIU Receive Impedance and Sensitivity Monitor Register**
 Register Address: **1007h + (20h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|---------|--------|--------|-----|--------|-------|-------|
| Name | RG703 | RIMPOFF | RIMPM1 | RIMPM0 | RTR | RMONEN | RSMS1 | RSMS0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive G.703 Clock Enable (RG703). If this bit is set, the receiver expects a 2.048MHz or 1.544MHz clock from the RTIP/RRING, based on the selection of T1 (1.544) or E1 (2.048) mode in the [LTRCR](#) register.

Bit 6: Receive Impedance Termination Off (RIMPOFF).
 0 = Receive terminating impedance match is enabled.
 1 = Receive terminating impedance match is disabled.

Bits 5 and 4: Receive Impedance Match 1 and 0 (RIMPM[1:0]). These bits are used to select the receive impedance match value. These must be set according to the cable impedance. Even if the internal receive match impedance is turned off (RIMPOFF); the external cable impedance must be specified for optimum operation by RIMPM1 to 0. See [Table 9-18](#).

Bit 3: Receiver Turns Ratio (RTR).
 0 = Receive transformer turns ratio is 1:1.
 1 = Receive transformer turns ratio is 2:1. This option should only be used in short-haul applications.

Bit 2: Receiver Monitor Mode Enable (RMONEN).
 0 = Disable receive monitor mode.
 1 = Enable receive monitor mode. Resistive gain is added with the maximum sensitivity. The receiver sensitivity is determined by RSMS1 and RSMS0.

Bits 1 and 0: Receiver Sensitivity/Monitor Gain Select 1 and 0 (RSMS[1:0]). These bits are used to select the receiver sensitivity level and additional gain in monitoring applications. The monitor mode (RMONEN) adds resistive gain to compensate for the signal loss caused by the isolation resistors. See [Table 9-19](#) and [Table 9-20](#).

Table 9-18. Receive Impedance Selection

| RIMPM[1:0] | RECEIVE IMPEDANCE SELECTED (Ω) |
|------------|--|
| 00 | 75 |
| 01 | 100 |
| 10 | 110 |
| 11 | 120 |

Table 9-19. Receiver Sensitivity Selection with Monitor Mode Disabled

| RMONEN | RSMS[1:0] | RECEIVER MONITOR MODE GAIN (dB) | RECEIVER SENSITIVITY (MAX CABLE LOSS ALLOWED) (dB) |
|---------------|------------------|--|---|
| 0 | 00 | 0 | 12 |
| 0 | 01 | 0 | 18 |
| 0 | 10 | 0 | 30 |
| 0 | 11 | 0 | 36 for T1; 43 for E1 |

Table 9-20. Receiver Sensitivity Selection with Monitor Mode Enabled

| RMONEN | RSMS[1:0] | RECEIVER MONITOR MODE GAIN (dB) | RECEIVER SENSITIVITY (MAX CABLE LOSS ALLOWED) (dB) |
|---------------|------------------|--|---|
| 1 | 00 | 14 | 30 |
| 1 | 01 | 20 | 22.5 |
| 1 | 10 | 26 | 17.5 |
| 1 | 11 | 32 | 12 |

9.6 BERT Register Definitions

Table 9-21. BERT Register Set

| ADDR | NAME | DESCRIPTION | R/W |
|-------|----------------------|---|-----|
| 1100h | BAWC | BERT Alternating Word Count Rate Register | R |
| 1101h | BRP1 | BERT Repetitive Pattern Set Register 1 | R/W |
| 1102h | BRP2 | BERT Repetitive Pattern Set Register 2 | R/W |
| 1103h | BRP3 | BERT Repetitive Pattern Set Register 3 | R/W |
| 1104h | BRP4 | BERT Repetitive Pattern Set Register 4 | R/W |
| 1105h | BC1 | BERT Control Register 1 | R/W |
| 1106h | BC2 | BERT Control Register 2 | R/W |
| 1107h | BBC1 | BERT Bit Count Register 1 | R |
| 1108h | BBC2 | BERT Bit Count Register 2 | R |
| 1109h | BBC3 | BERT Bit Count Register 3 | R |
| 110Ah | BBC4 | BERT Bit Count Register 4 | R |
| 110Bh | BEC1 | BERT Error Count Register 1 | R |
| 110Ch | BEC2 | BERT Error Count Register 2 | R |
| 110Dh | BEC3 | BERT Error Count Register 3 | R |
| 110Eh | BLSR | BERT Latched Status Register | R |
| 110Fh | BSIM | BERT Status Interrupt Mask Register | R/W |

Register Name: **BAWC**
 Register Description: **BERT Alternating Word Count Rate Register**
 Register Address: **1100h + (10h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | ACNT7 | ACNT6 | ACNT5 | ACNT4 | ACNT3 | ACNT2 | ACNT1 | ACNT0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Alternating Word Count Rate Bits 7 to 0 (ACNT[7:0]). When the BERT is programmed in the alternating word mode, the words will repeat for the count loaded into this register, then flip to the other word and again repeat for the number of times loaded into this register. ACNT0 is the LSB of the 8-bit alternating word count rate counter.

Register Name: **BRP1**
 Register Description: **BERT Repetitive Pattern Set Register 1**
 Register Address: **1101h + (10h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | RPAT7 | RPAT6 | RPAT5 | RPAT4 | RPAT3 | RPAT2 | RPAT1 | RPAT0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: BERT Repetitive Pattern Set Bits 7 to 0 (RPAT[7:0]). RPAT0 is the LSB of the 32-bit repetitive pattern.

Register Name: **BRP2**
 Register Description: **BERT Repetitive Pattern Set Register 2**
 Register Address: **1102h + (10h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|-------|-------|
| Name | RPAT15 | RPAT14 | RPAT13 | RPAT12 | RPAT11 | RPAT10 | RPAT9 | RPAT8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: BERT Repetitive Pattern Set Bits 15 to 8 (RPAT[15:8]).

Register Name: **BRP3**
 Register Description: **BERT Repetitive Pattern Set Register 3**
 Register Address: **1103h + (10h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Name | RPAT23 | RPAT22 | RPAT21 | RPAT20 | RPAT19 | RPAT18 | RPAT17 | RPAT16 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: BERT Repetitive Pattern Set Bits 23 to 16 (RPAT[23:16]).

Register Name: **BRP4**
 Register Description: **BERT Repetitive Pattern Set Register 4**
 Register Address: **1104h + (10h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Name | RPAT31 | RPAT30 | RPAT29 | RPAT28 | RPAT27 | RPAT26 | RPAT25 | RPAT24 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: BERT Repetitive Pattern Set Bits 31 to 24 (RPAT[31:24]). RPAT31 is the MSB of the 32-bit repetitive pattern.

Register Name: **BC1**
 Register Description: **BERT Control Register 1**
 Register Address: **1105h + (10h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|------|------|-----|-----|-----|----|--------|
| Name | TC | TINV | RINV | PS2 | PS1 | PS0 | LC | RESYNC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit Pattern Load (TC). A low-to-high transition loads the pattern generator with the pattern that is to be generated. This bit should be toggled from low to high whenever the host wishes to load a new pattern. Must be cleared and set again for subsequent loads.

Bit 6: Transmit Invert Data Enable (TINV).

0 = do not invert the outgoing data stream
 1 = invert the outgoing data stream

Bit 5: Receive Invert Data Enable (RINV).

0 = do not invert the incoming data stream
 1 = invert the incoming data stream

Bits 4 to 2: Pattern Select Bits 2 to 0 (PS[2:0]). These bits select data pattern used by the transmit and receive circuits. See [Table 9-22](#).

Table 9-22. BERT Pattern Select

| PS2 | PS1 | PS0 | PATTERN DEFINITION |
|-----|-----|-----|---|
| 0 | 0 | 0 | Pseudorandom 2E7-1 |
| 0 | 0 | 1 | Pseudorandom 2E11-1 |
| 0 | 1 | 0 | Pseudorandom 2E15-1 |
| 0 | 1 | 1 | Pseudorandom Pattern QRSS. A $2^{20} - 1$ pattern with 14 consecutive zero restriction. |
| 1 | 0 | 0 | Repetitive Pattern |
| 1 | 0 | 1 | Alternating Word Pattern |
| 1 | 1 | 0 | Modified 55 Octet (Daly) Pattern. The Daly pattern is a repeating 55 octet pattern that is byte-aligned into the active DS0 time slots. The pattern is defined in an ATIS (Alliance for Telecommunications Industry Solutions) Committee T1 Technical Report Number 25 (November 1993). |
| 1 | 1 | 1 | Pseudorandom 2E-9-1 |

Bit 1: Load Bit and Error Counter (LC). A low-to-high transition latches the current bit and error counts into the registers [BBC1](#), [BBC2](#), [BBC3](#), [BBC4](#) and [BEC1](#), [BEC2](#), and [BEC3](#), and clears the internal count. This bit should be toggled from low to high whenever the host wishes to begin a new acquisition period. Must be cleared and set again for subsequent loads.

Bit 0: Force Resynchronization (RESYNC). A low-to-high transition forces the receive BERT synchronizer to resynchronize to the incoming data stream. This bit should be toggled from low to high whenever the host wishes to acquire synchronization on a new pattern. Must be cleared and set again for a subsequent resynchronization.

Register Name: **BC2**
 Register Description: **BERT Control Register 2**
 Register Address: **1106h + (10h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|-----|------|------|------|------|
| Name | EIB2 | EIB1 | EIB0 | SBE | RPL3 | RPL2 | RPL1 | RPL0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 5: Error Insert Bits 2 to 0 (EIB[2:0]). Will automatically insert bit errors at the prescribed rate into the generated data pattern. Can be used for verifying error detection features. See [Table 9-23](#).

Table 9-23. BERT Error Insertion Rate

| EIB2 | EIB1 | EIB0 | ERROR RATE INSERTED |
|------|------|------|----------------------------------|
| 0 | 0 | 0 | No errors automatically inserted |
| 0 | 0 | 1 | 10E-1 |
| 0 | 1 | 0 | 10E-2 |
| 0 | 1 | 1 | 10E-3 |
| 1 | 0 | 0 | 10E-4 |
| 1 | 0 | 1 | 10E-5 |
| 1 | 1 | 0 | 10E-6 |
| 1 | 1 | 1 | 10E-7 |

Bit 4: Single Bit Error Insert (SBE). A low-to-high transition will create a single bit error. Must be cleared and set again for a subsequent bit error to be inserted.

Bits 3 to 0: Repetitive Pattern Length Select 3 to 0 (RPL[3:0]). RPL0 is the LSB and RPL3 is the MSB of a nibble that describes how long the repetitive pattern is. The valid range is 17 (0000) to 32 (1111). These bits are ignored if the receive BERT is programmed for a pseudorandom pattern. To create repetitive patterns fewer than 17 bits in length, the user must set the length to an integer number of the desired length that is less than or equal to 32. For example, to create a 6-bit pattern, the user can set the length to 18 (0001) or to 24 (0111) or to 30 (1101). See [Table 9-24](#).

Table 9-24. BERT Repetitive Pattern Length Select

| LENGTH (BITS) | RPL3 | RPL2 | RPL1 | RPL0 |
|---------------|------|------|------|------|
| 17 | 0 | 0 | 0 | 0 |
| 18 | 0 | 0 | 0 | 1 |
| 19 | 0 | 0 | 1 | 0 |
| 20 | 0 | 0 | 1 | 1 |
| 21 | 0 | 1 | 0 | 0 |
| 22 | 0 | 1 | 0 | 1 |
| 23 | 0 | 1 | 1 | 0 |
| 24 | 0 | 1 | 1 | 1 |
| 25 | 1 | 0 | 0 | 0 |
| 26 | 1 | 0 | 0 | 1 |
| 27 | 1 | 0 | 1 | 0 |
| 28 | 1 | 0 | 1 | 1 |
| 29 | 1 | 1 | 0 | 0 |
| 30 | 1 | 1 | 0 | 1 |
| 31 | 1 | 1 | 1 | 0 |
| 32 | 1 | 1 | 1 | 1 |

Register Name: **BBC1**
 Register Description: **BERT Bit Count Register 1**
 Register Address: **1107h + (10h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | BBC7 | BBC6 | BBC5 | BBC4 | BBC3 | BBC2 | BBC1 | BBC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: BERT Bit Counter Bits 7 to 0 (BBC[7:0]). BBC0 is the LSB of the 32-bit counter.

Register Name: **BBC2**
 Register Description: **BERT Bit Count Register 2**
 Register Address: **1108h + (10h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|------|------|
| Name | BBC15 | BBC14 | BBC13 | BBC12 | BBC11 | BBC10 | BBC9 | BBC8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: BERT Bit Counter Bits 15 to 8 (BBC[15:8]).

Register Name: **BBC3**
 Register Description: **BERT Bit Count Register 3**
 Register Address: **1109h + (10h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | BBC23 | BBC22 | BBC21 | BBC20 | BBC19 | BBC18 | BBC17 | BBC16 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: BERT Bit Counter Bits 23 to 16 (BBC[23:16]).

Register Name: **BBC4**
 Register Description: **BERT Bit Count Register 4**
 Register Address: **110Ah + (10h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | BBC31 | BBC30 | BBC29 | BBC28 | BBC27 | BBC26 | BBC25 | BBC24 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: BERT Bit Counter Bits 31 to 24 (BBC[31:24]). BBC31 is the MSB of the 32-bit counter.

Register Name: **BEC1**
 Register Description: **BERT Error Count Register 1**
 Register Address: **110Bh + (10h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | EC7 | EC6 | EC5 | EC4 | EC3 | EC2 | EC1 | EC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Error Counter Bits 7 to 0 (EC[7:0]). EC0 is the LSB of the 24-bit counter.

Register Name: **BEC2**
 Register Description: **BERT Error Count Register 2**
 Register Address: **110Ch + (10h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|-----|-----|
| Name | EC15 | EC14 | EC13 | EC12 | EC11 | EC10 | EC9 | EC8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Error Counter Bits 15 to 8 (EC[15:8]).

Register Name: **BEC3**
 Register Description: **BERT Error Count Register 3**
 Register Address: **110Dh + (10h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | EC23 | EC22 | EC21 | EC20 | EC19 | EC18 | EC17 | EC16 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Error Counter Bits 23 to 16 (EC[23:16]). EC23 is the MSB of the 24-bit counter.

Register Name: **BLSR**
 Register Description: **BERT Latched Status Register**
 Register Address: **110Eh + (10h x n); where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|------|------|------|------|------|-------|-------|
| Name | — | BBED | BBCO | BECO | BRA1 | BRA0 | BRLOS | BSYNC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are latched and can create interrupts.

Bit 6: BERT Bit-Error-Detected Event (BBED). A latched bit that is set when a bit error is detected. The receive BERT must be in synchronization for it to detect bit errors.

Bit 5: BERT Bit Counter Overflow Event (BBCO). A latched bit that is set when the 32-bit BERT bit counter (BBC) overflows.

Bit 4: BERT Error Counter Overflow Event (BECO). A latched bit that is set when the 24-bit BERT error counter (BEC) overflows.

Bit 3: BERT Receive All-Ones Condition (BRA1). A latched bit that is set when 32 consecutive ones are received.

Bit 2: BERT Receive All-Zeros Condition (BRA0). A latched bit that is set when 32 consecutive zeros are received.

Bit 1: BERT Receive Loss of Synchronization Condition (BRLOS). A latched bit that is set whenever the receive BERT begins searching for a pattern.

Bit 0: BERT in Synchronization Condition (BSYNC). Will be set when the incoming pattern matches for 32 consecutive bit positions.

Register Name: **BSIM**
 Register Description: **BERT Status Interrupt Mask Register**
 Register Address: **110Fh + (10h x n): where n = 0 to 3, for Ports 1 to 4**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|------|------|------|------|------|-------|-------|
| Name | — | BBED | BBCO | BECO | BRA1 | BRA0 | BRLOS | BSYNC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 6: BERT Bit-Error-Detected Event (BBED).

0 = interrupt masked
 1 = interrupt enabled

Bit 5: BERT Bit Counter Overflow Event (BBCO).

0 = interrupt masked
 1 = interrupt enabled

Bit 4: BERT Error Counter Overflow Event (BECO).

0 = interrupt masked
 1 = interrupt enabled

Bit 3: BERT Receive All-Ones Condition (BRA1).

0 = interrupt masked
 1 = interrupt enabled—interrupts on rising and falling edges

Bit 2: BERT Receive All-Zeros Condition (BRA0).

0 = interrupt masked
 1 = interrupt enabled—interrupts on rising and falling edges

Bit 1: BERT Receive Loss of Synchronization Condition (BRLOS)

0 = interrupt masked
 1 = interrupt enabled—interrupts on rising and falling edges

Bit 0: BERT in Synchronization Condition (BSYNC).

0 = interrupt masked
 1 = interrupt enabled—interrupts on rising and falling edges

10. FUNCTIONAL TIMING

10.1 T1 Receiver Functional Timing Diagrams

Figure 10-1. T1 Receive-Side D4 Timing

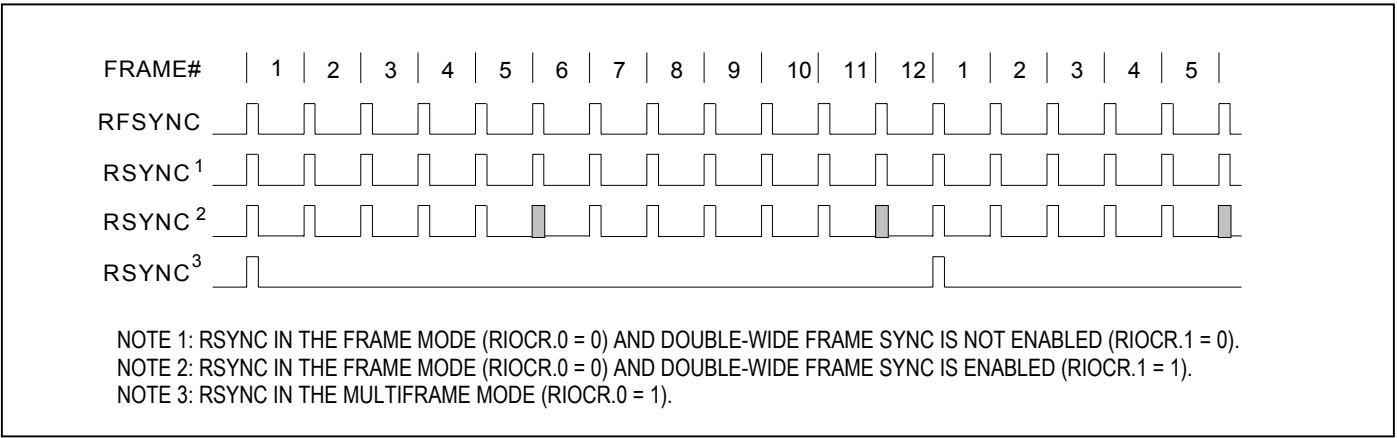


Figure 10-2. T1 Receive-Side ESF Timing

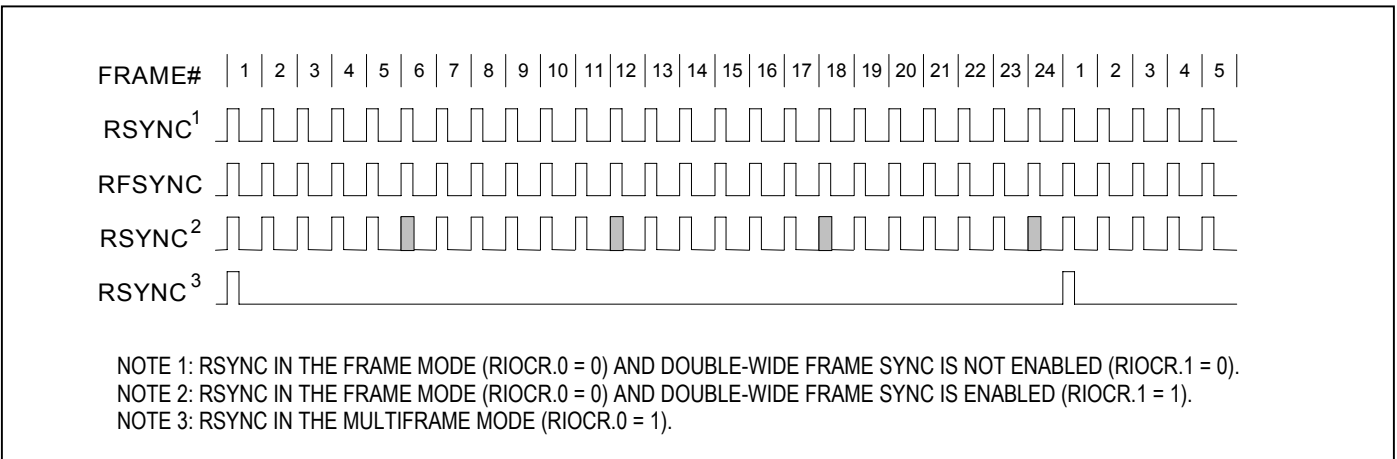


Figure 10-3. T1 Receive-Side Boundary Timing (Elastic Store Disabled)

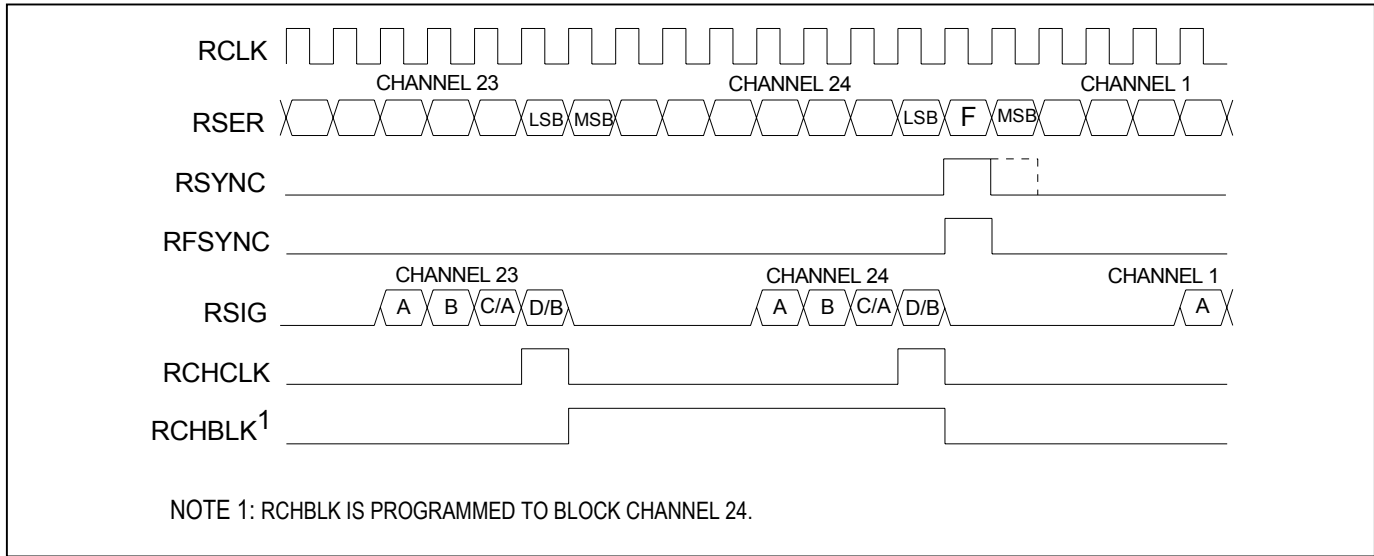


Figure 10-4. T1 Receive-Side 1.544MHz Boundary Timing (Elastic Store Enabled)

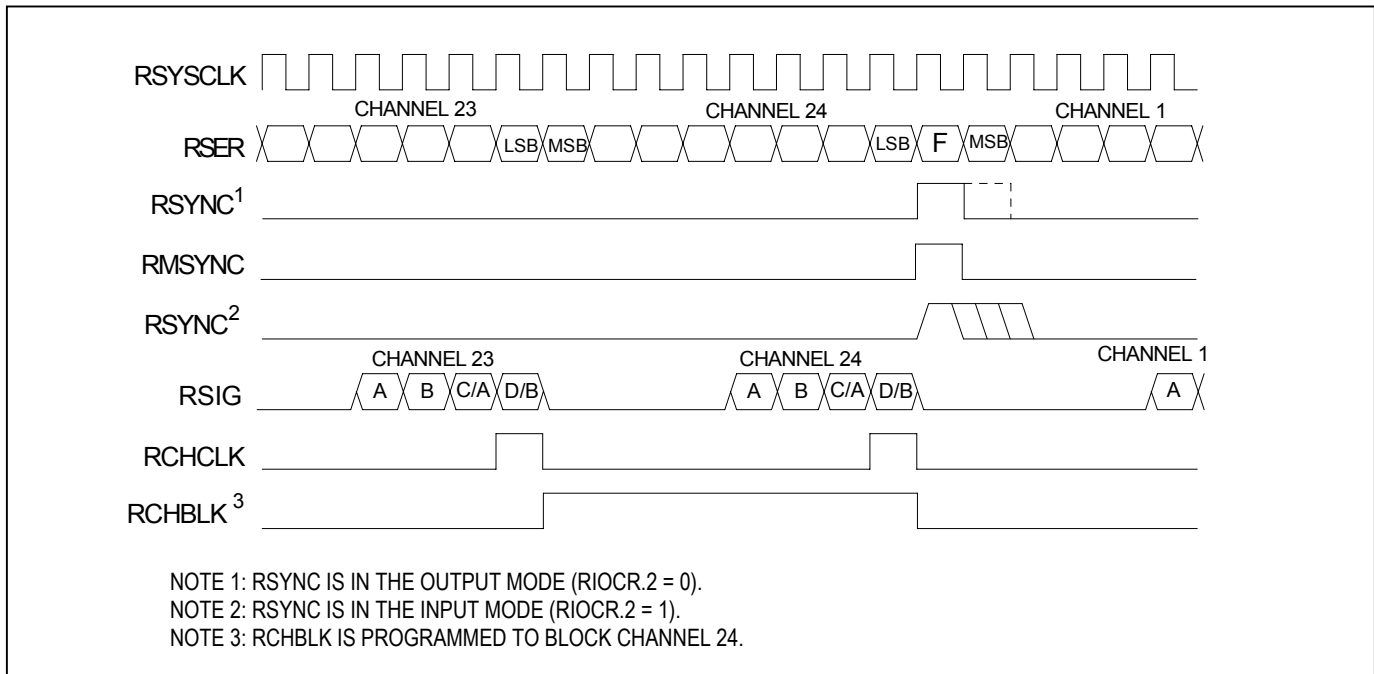
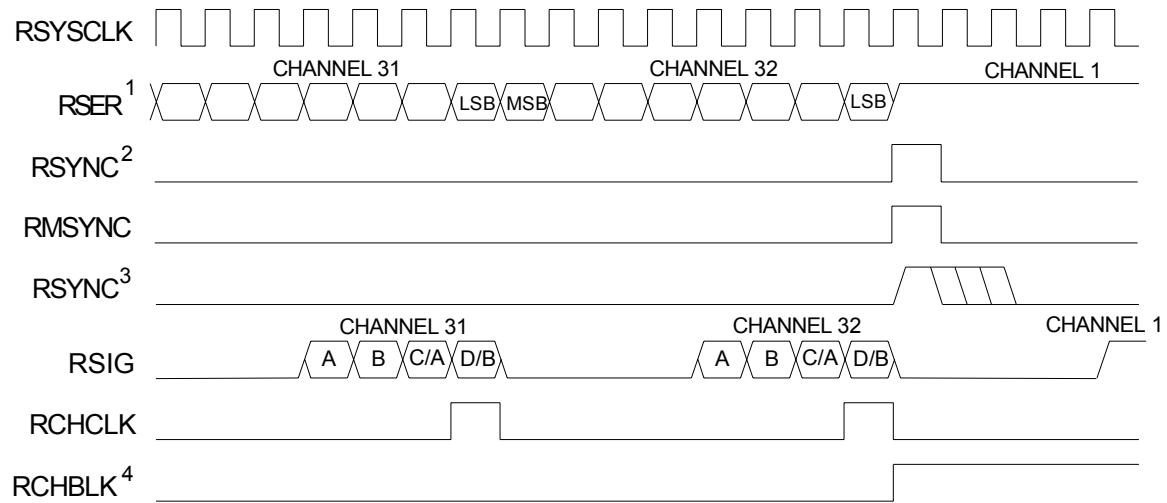


Figure 10-5. T1 Receive-Side 2.048MHz Boundary Timing (Elastic Store Enabled)

NOTE 1: RSER DATA IN CHANNELS 1, 5, 9, 13, 17, 21, 25, AND 29 ARE FORCED TO ONE.

NOTE 2: RSYNC IS IN THE OUTPUT MODE (RIOCR.2 = 0).

NOTE 3: RSYNC IS IN THE INPUT MODE (RIOCR.2 = 1).

NOTE 4: RCHBLK IS PROGRAMMED TO BLOCK CHANNEL 1.

NOTE 5: THE F-BIT POSITION IS PASSED THROUGH THE RECEIVE-SIDE ELASTIC STORE.

Figure 10-6. T1 Receive-Side Interleave Bus Operation—BYTE Mode

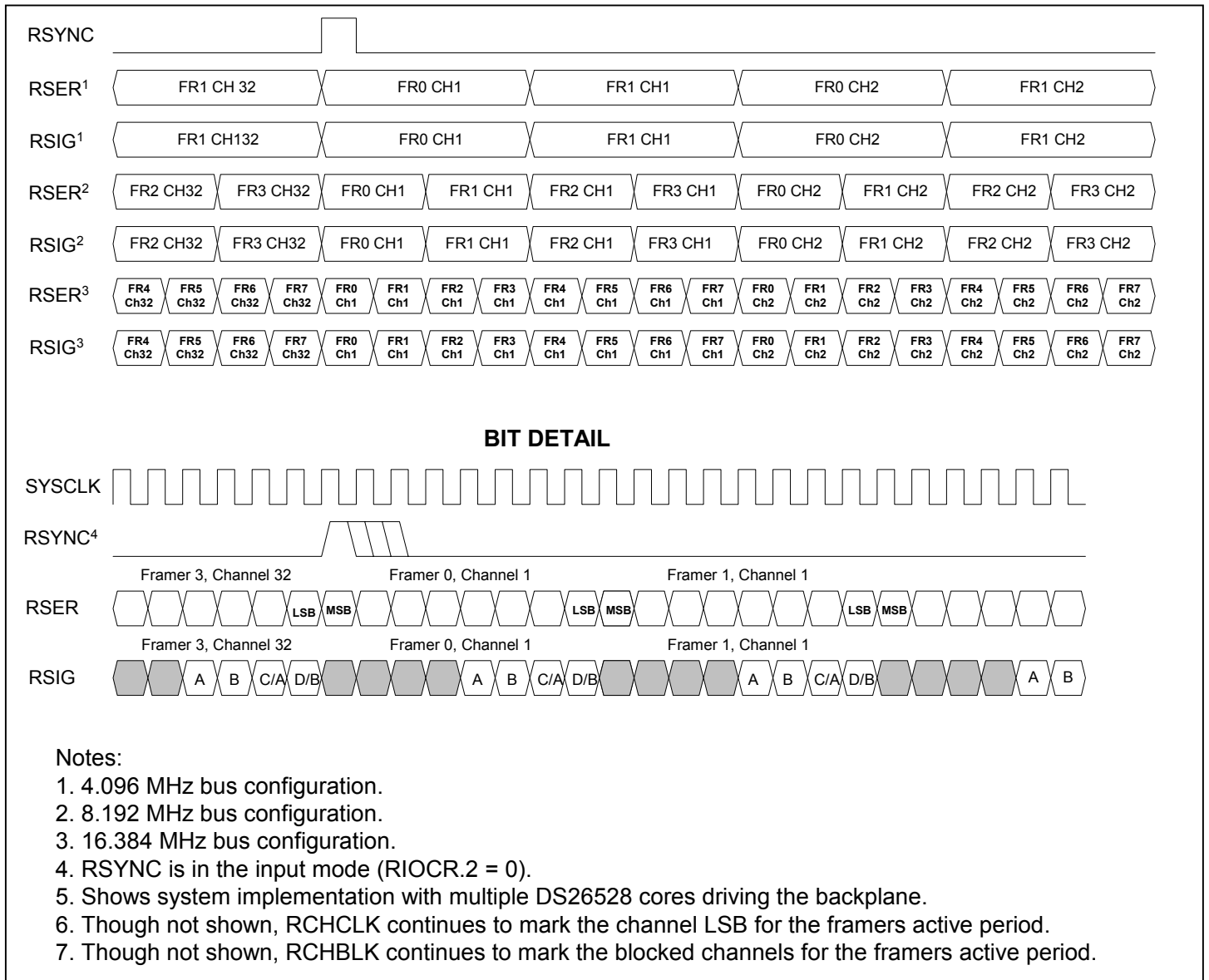
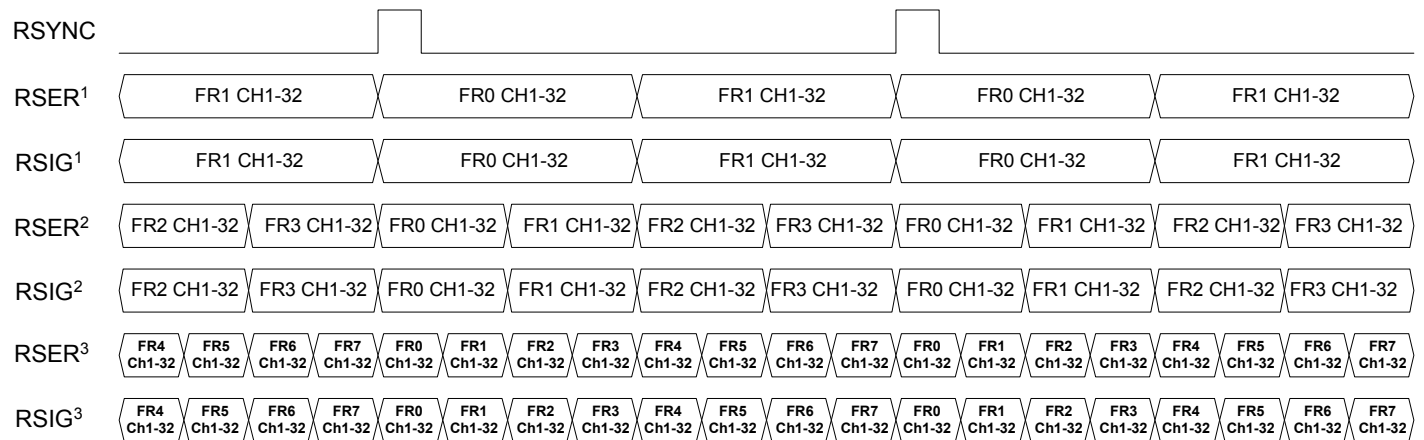
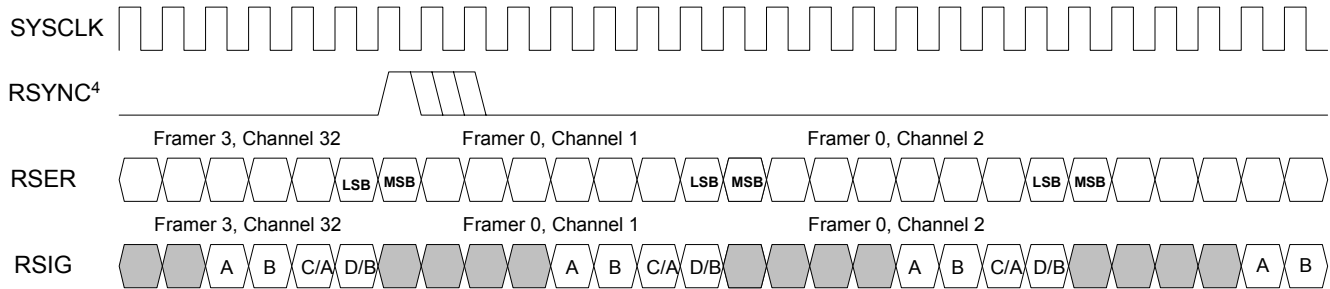


Figure 10-7. T1 Receive-Side Interleave Bus Operation—FRAME Mode



BIT DETAIL



Notes:

1. 4.096 MHz bus configuration.
2. 8.192 MHz bus configuration.
3. 16.384 MHz bus configuration.
4. RSYNC is in the input mode (RIOCR.2 = 0).
5. Shows system implementation with multiple DS26528 cores driving the backplane.
6. Though not shown, RCHCLK continues to mark the channel LSB for the framers active period.
7. Though not shown, RCHBLK continues to mark the blocked channels for the framers active period.

10.2 T1 Transmitter Functional Timing Diagrams

Figure 10-8. T1 Transmit-Side D4 Timing

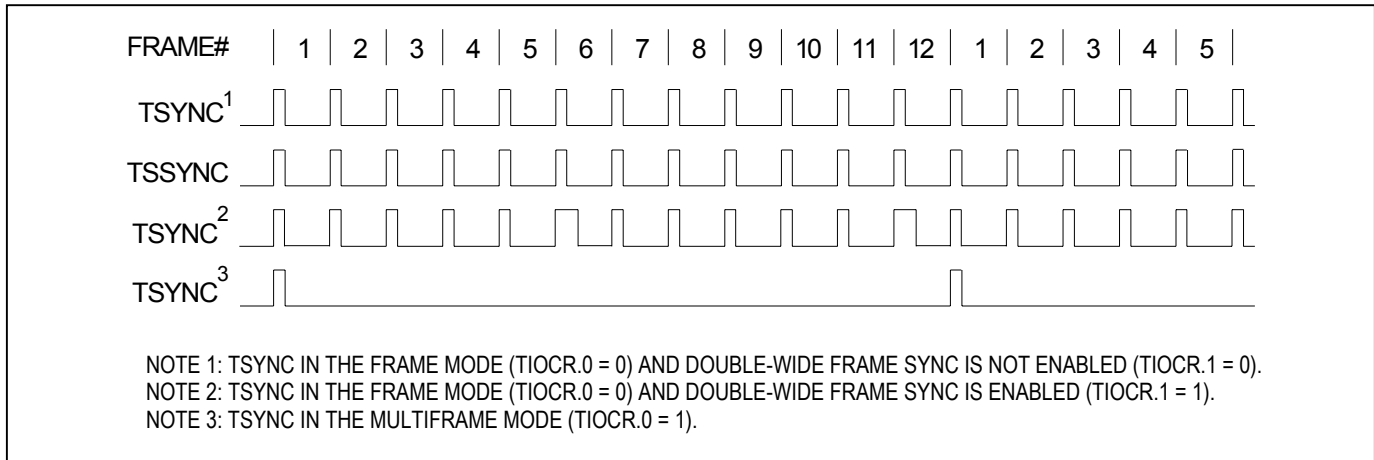


Figure 10-9. T1 Transmit-Side ESF Timing

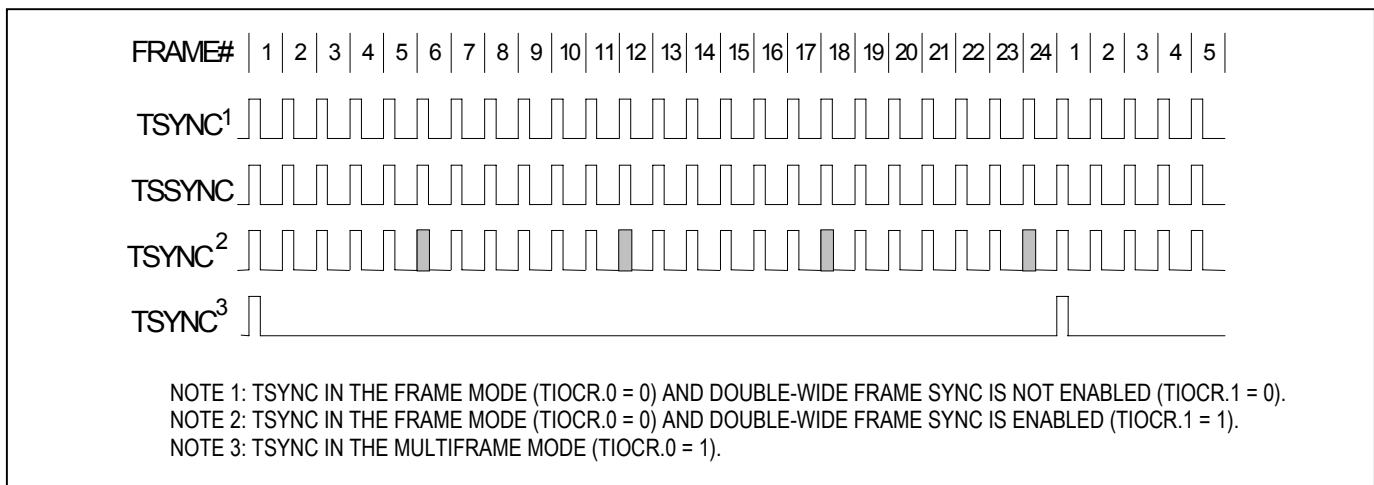


Figure 10-10. T1 Transmit-Side Boundary Timing (Elastic Store Disabled)

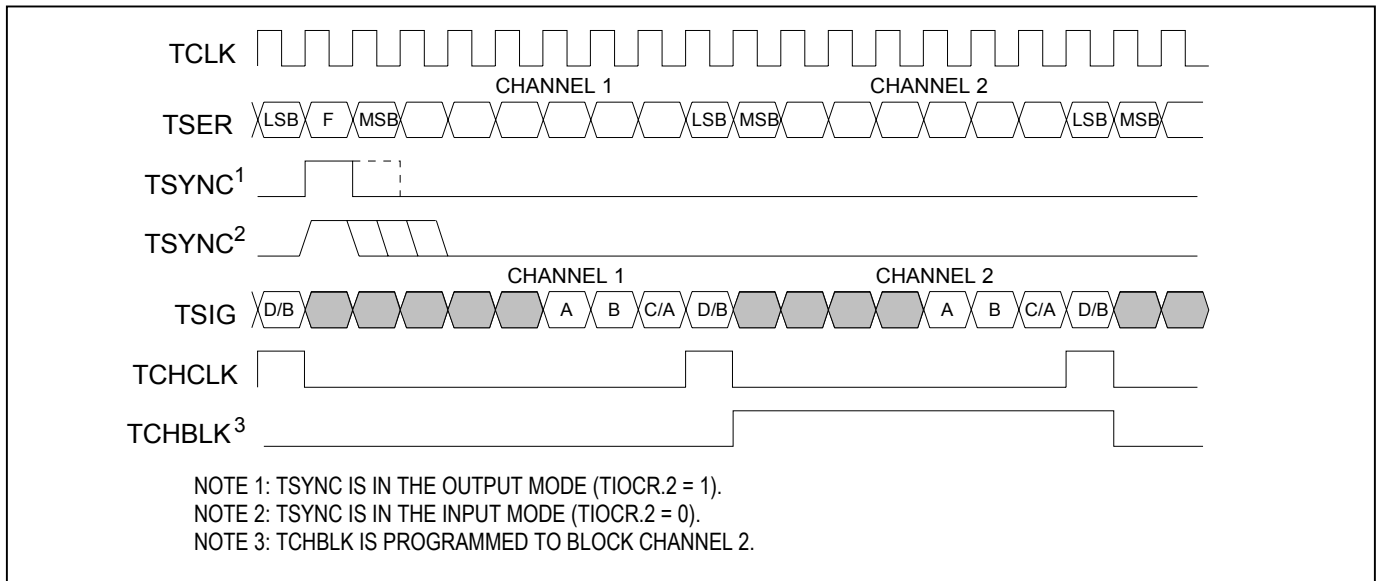


Figure 10-11. T1 Transmit-Side 1.544MHz Boundary Timing (Elastic Store Enabled)

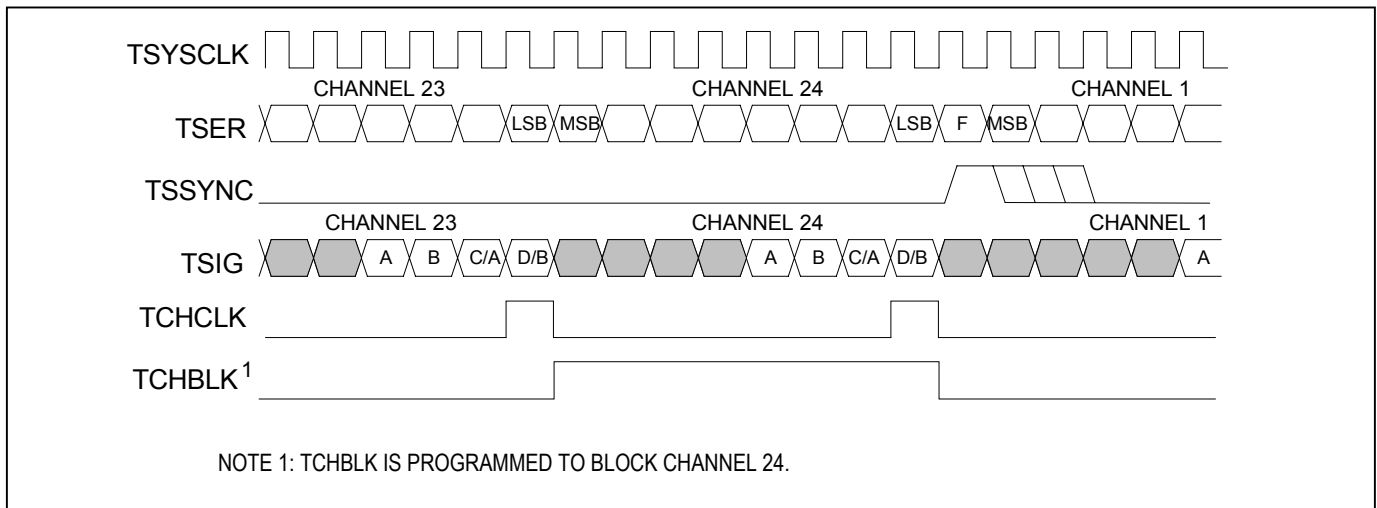
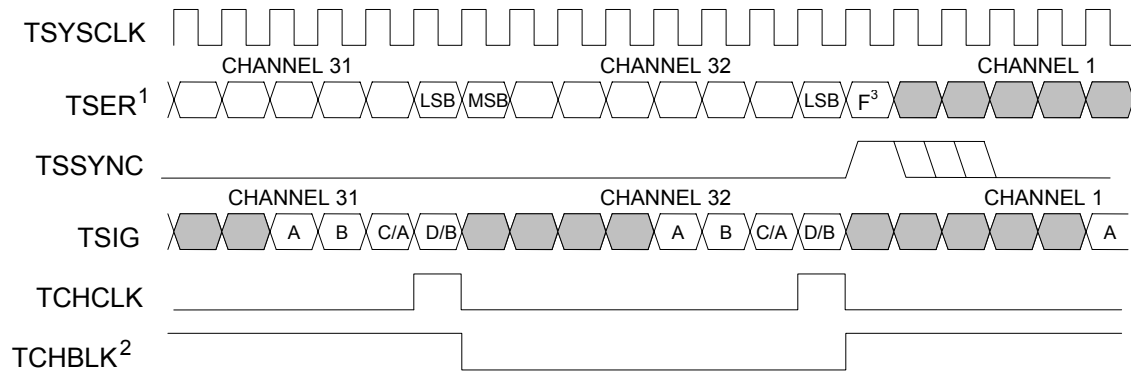


Figure 10-12. T1 Transmit-Side 2.048MHz Boundary Timing (Elastic Store Enabled)

NOTE 1: TSER DATA IN CHANNELS 1, 5, 9, 13, 17, 21, 25, AND 29 IS IGNORED.

NOTE 2: TCHBLK IS PROGRAMMED TO BLOCK CHANNELS 31 AND 1.

NOTE 3: THE F-BIT POSITION FOR THE T1 FRAME IS SAMPLED AND PASSED THROUGH THE TRANSMIT-SIDE ELASTIC STORE INTO THE MSB BIT POSITION OF CHANNEL 1. (NORMALLY THE TRANSMIT-SIDE FORMATTER OVERWRITES THE F-BIT POSITION UNLESS THE FORMATTER IS PROGRAMMED TO PASS THROUGH THE F-BIT POSITION).

Figure 10-13. T1 Transmit-Side Interleave Bus Operation—BYTE Mode

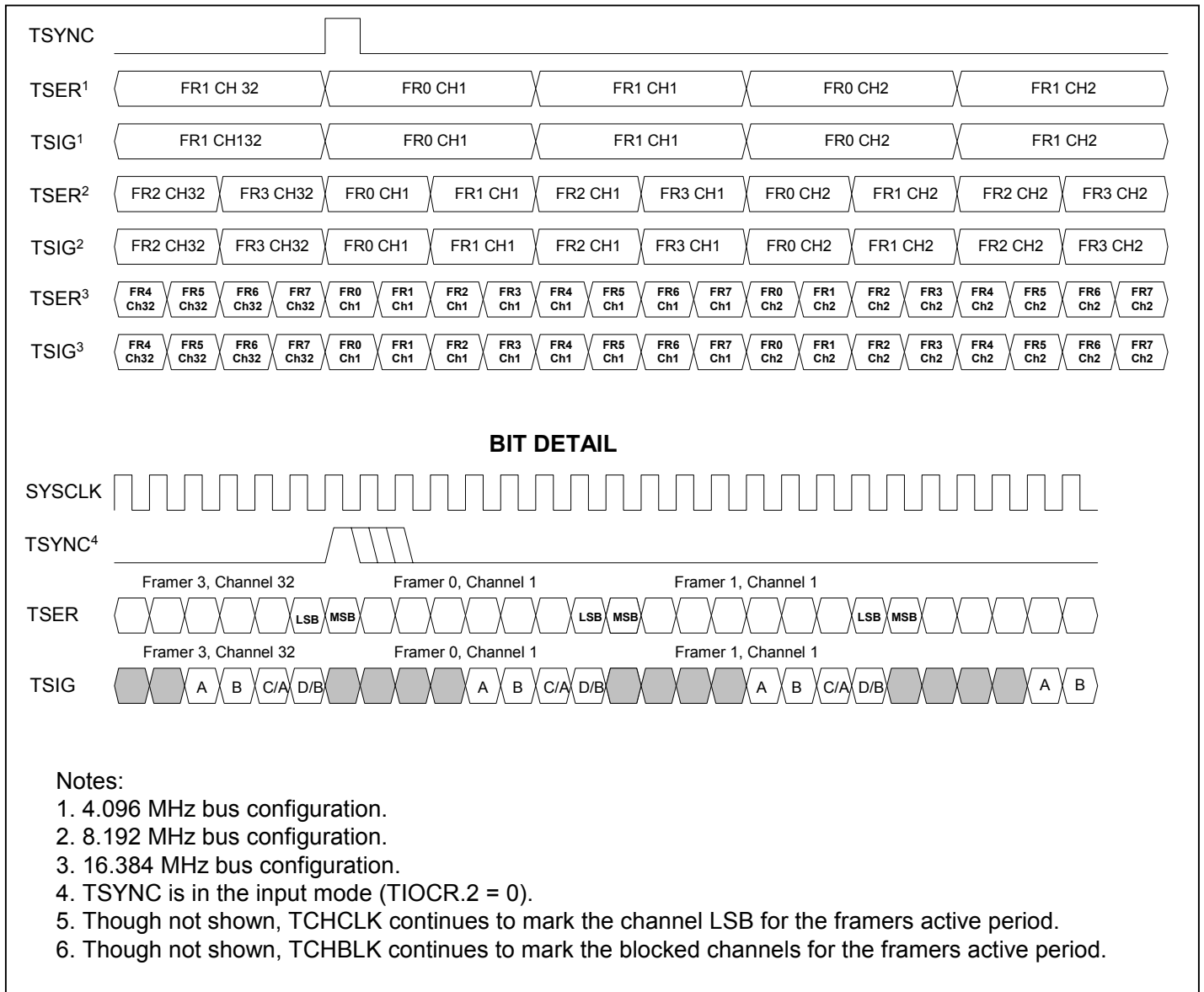
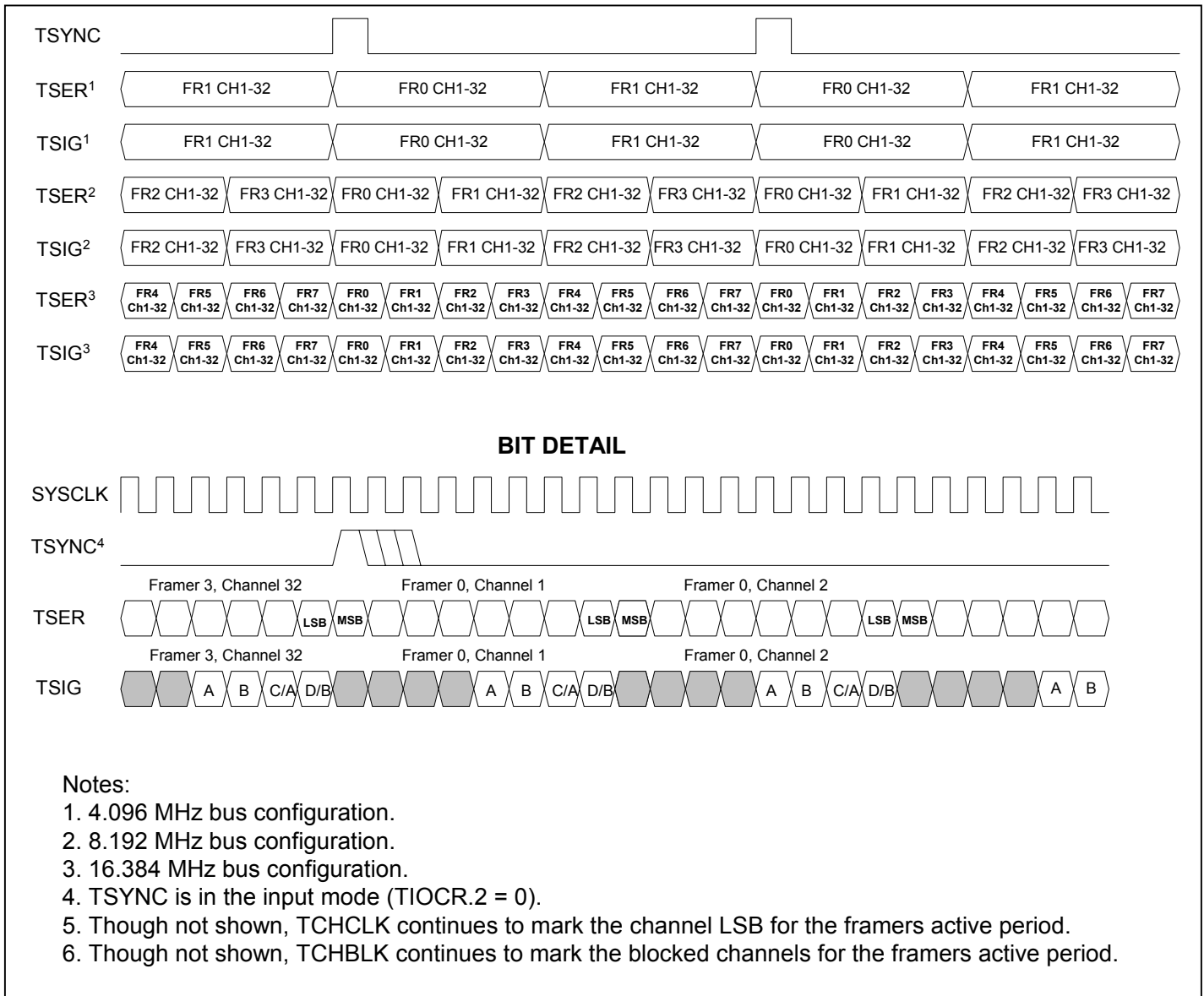


Figure 10-14. T1 Transmit Interleave Bus Operation—FRAME Mode



10.3 E1 Receiver Functional Timing Diagrams

Figure 10-15. E1 Receive-Side Timing

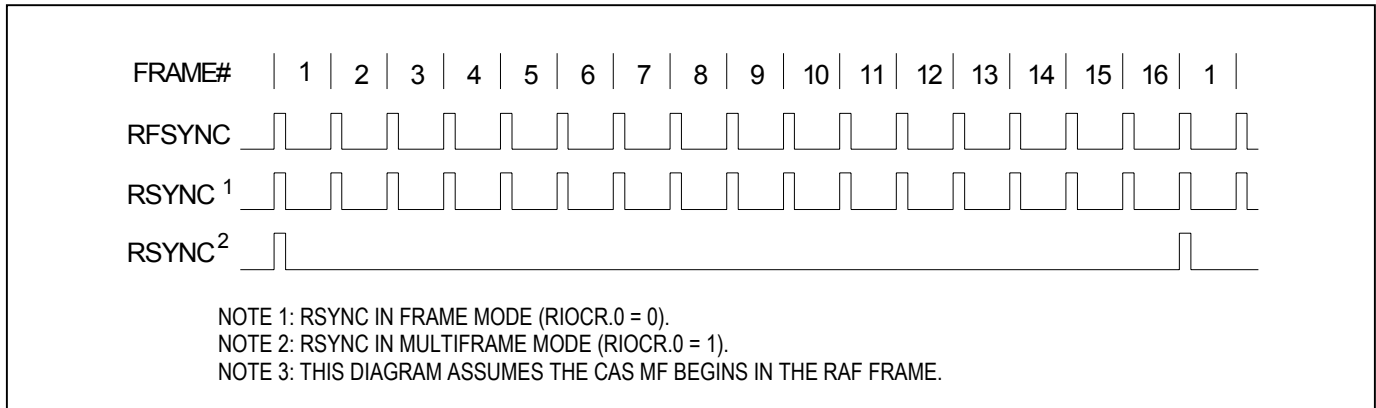


Figure 10-16. E1 Receive-Side Boundary Timing (Elastic Store Disabled)

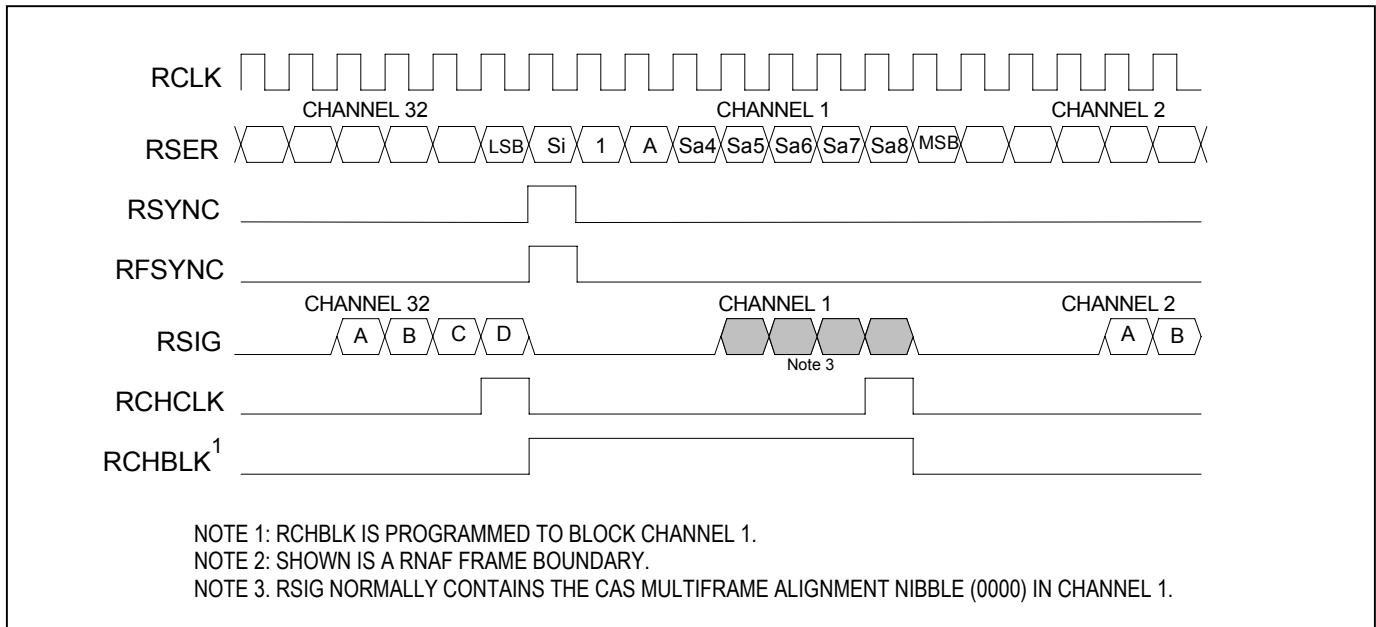


Figure 10-17. E1 Receive-Side 1.544MHz Boundary Timing (Elastic Store Enabled)

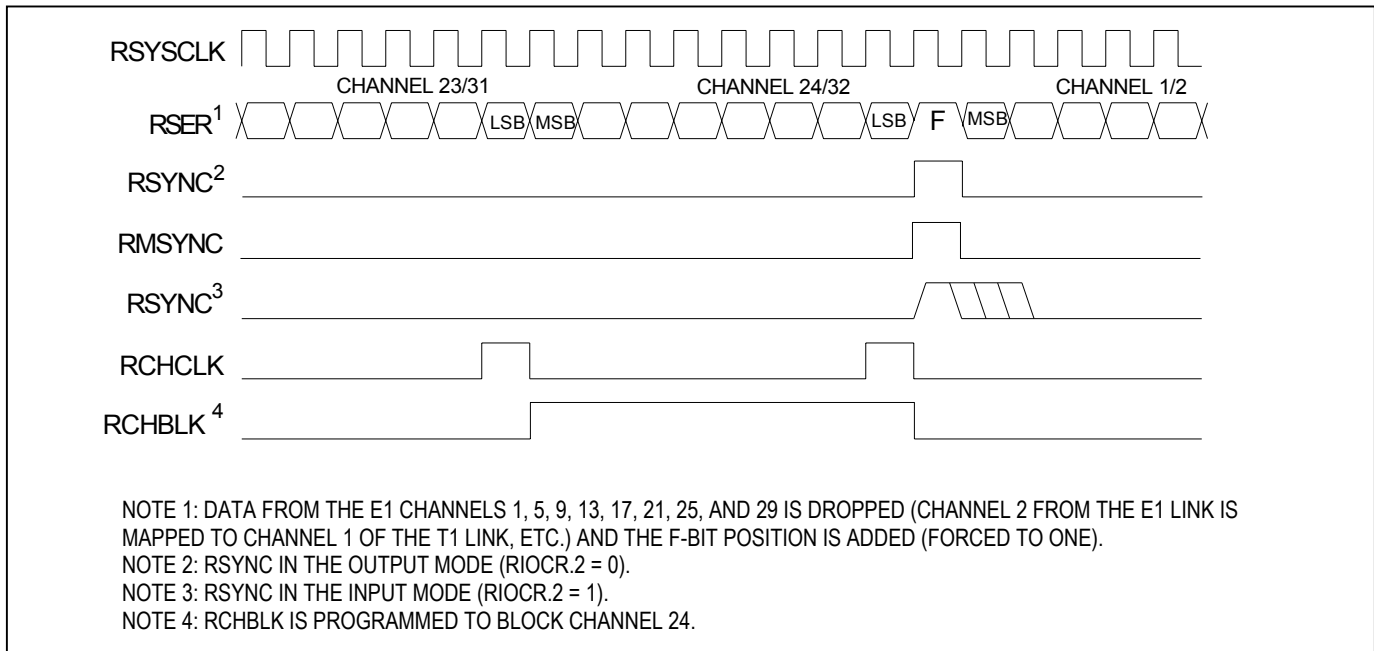
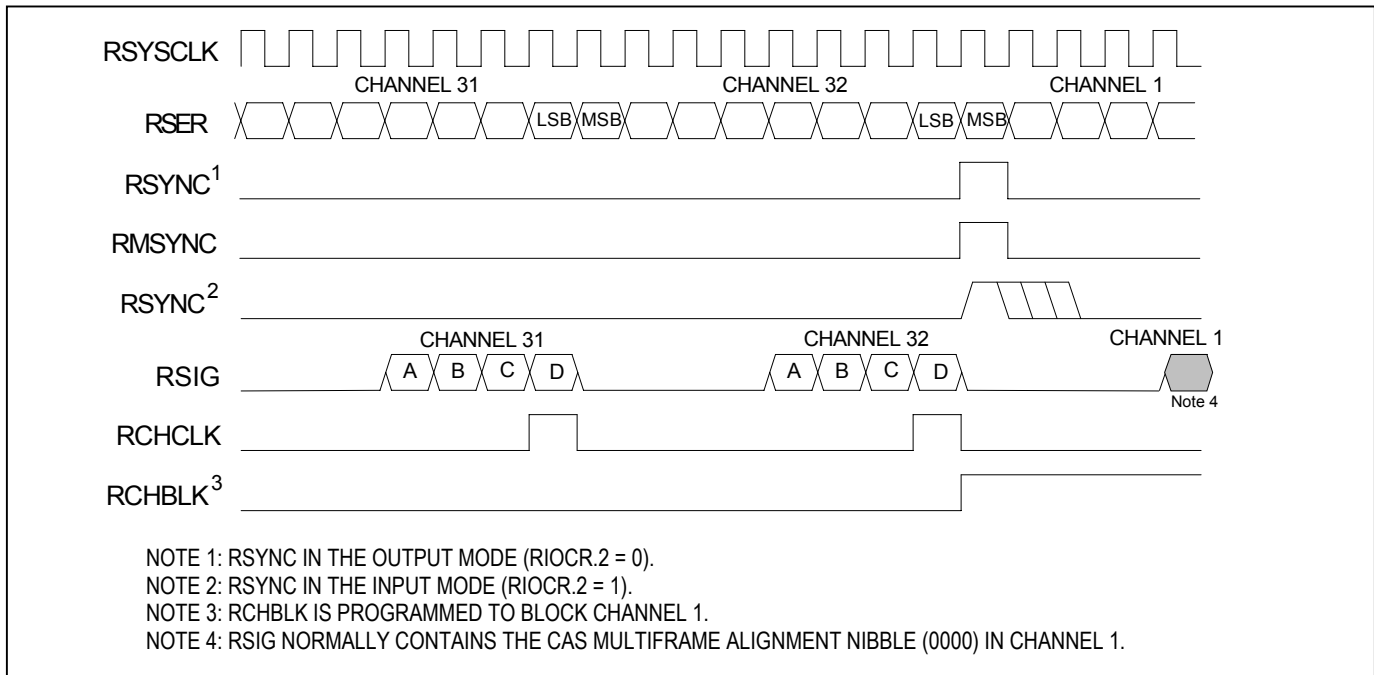


Figure 10-18. E1 Receive-Side 2.048MHz Boundary Timing (Elastic Store Enabled)



10.4 E1 Transmitter Functional Timing Diagrams

Figure 10-19. E1 Transmit-Side Timing

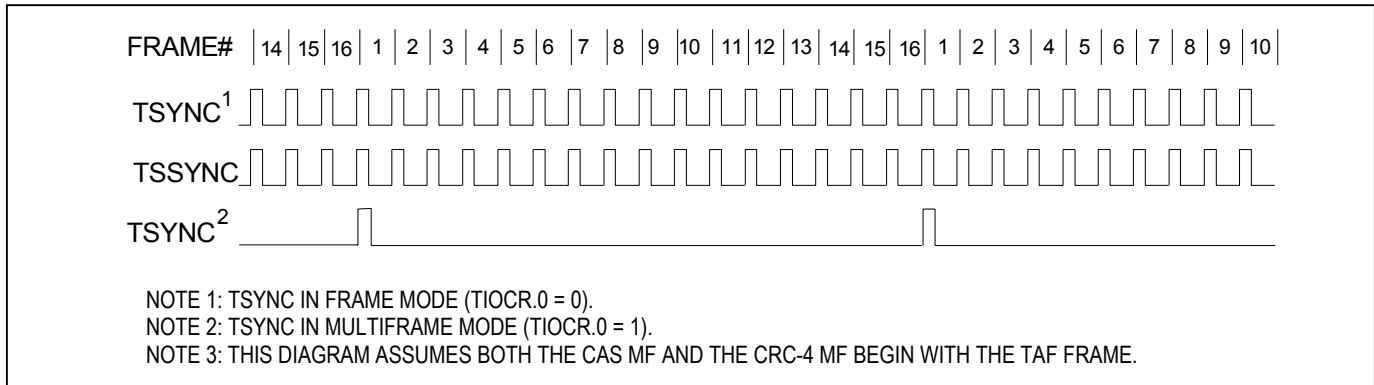


Figure 10-20. E1 Transmit-Side Boundary Timing (Elastic Store Disabled)

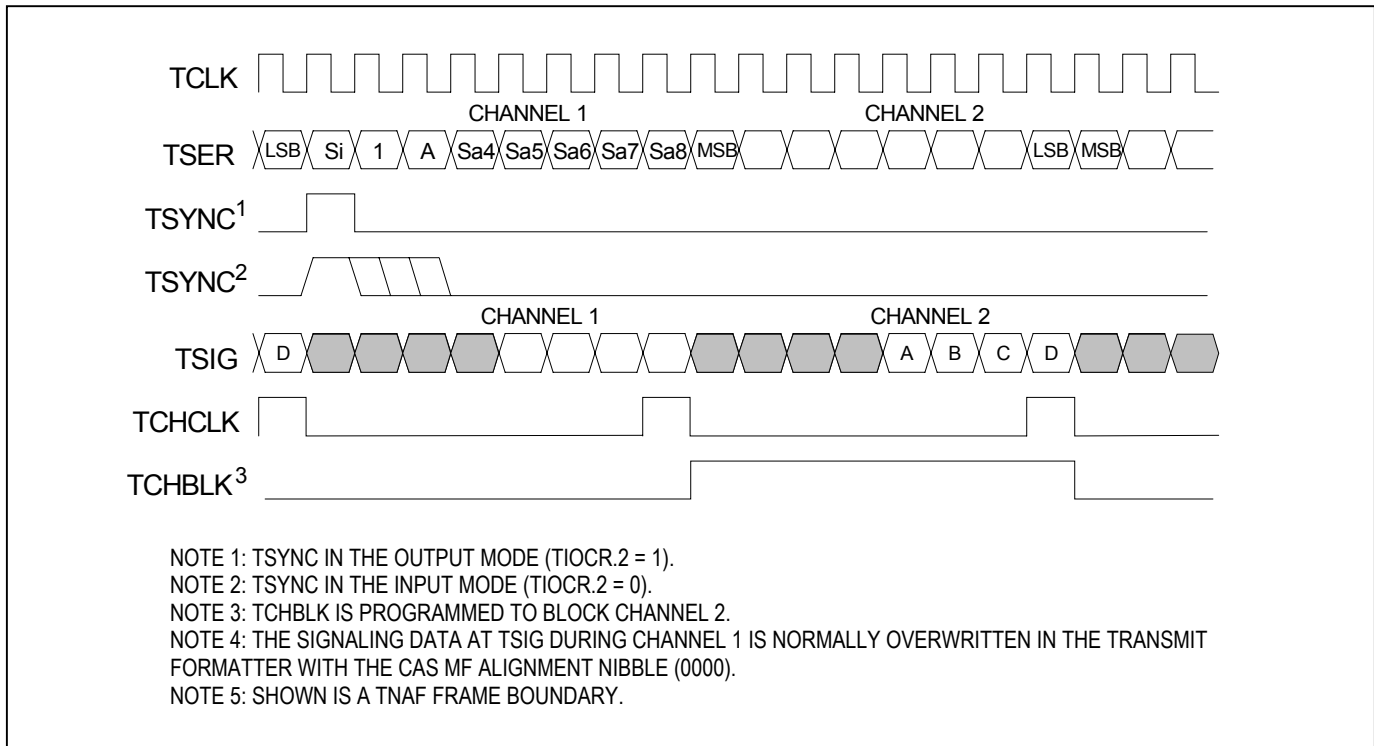


Figure 10-21. E1 Transmit-Side 1.544MHz Boundary Timing (Elastic Store Enabled)

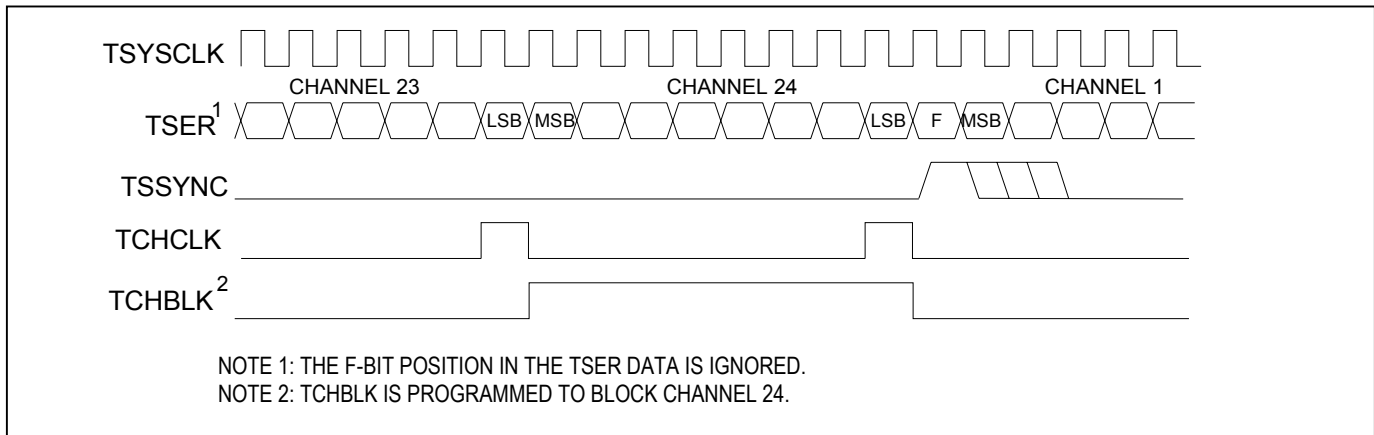


Figure 10-22. E1 Transmit-Side 2.048MHz Boundary Timing (Elastic Store Enabled)

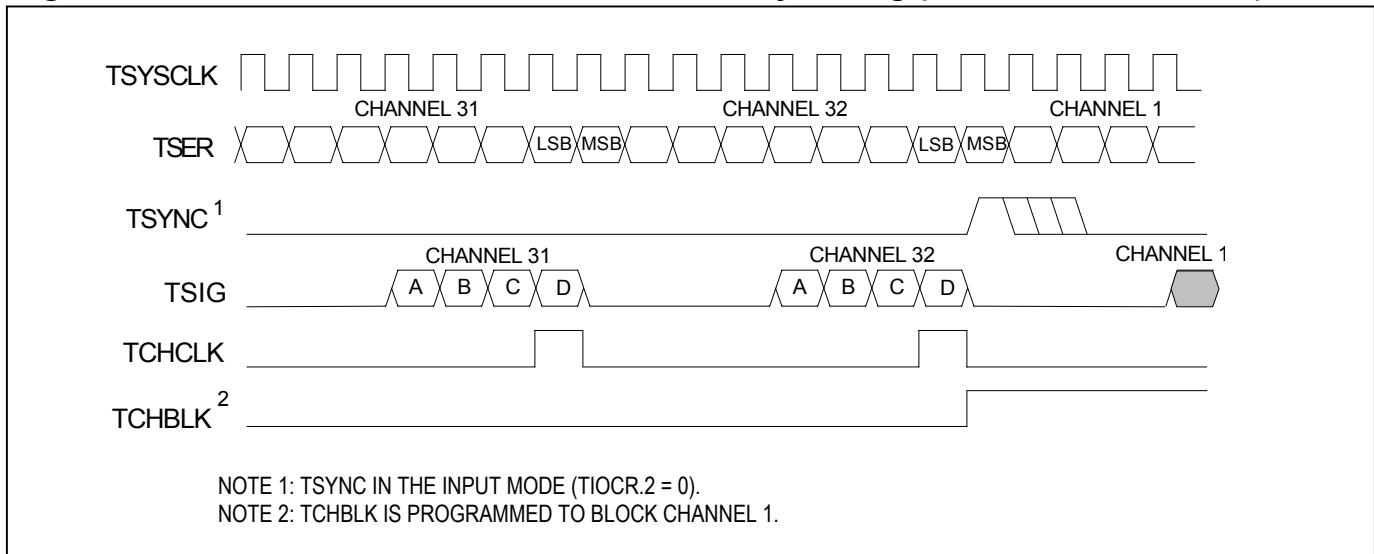
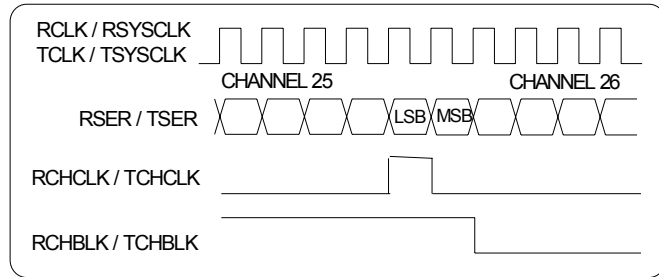
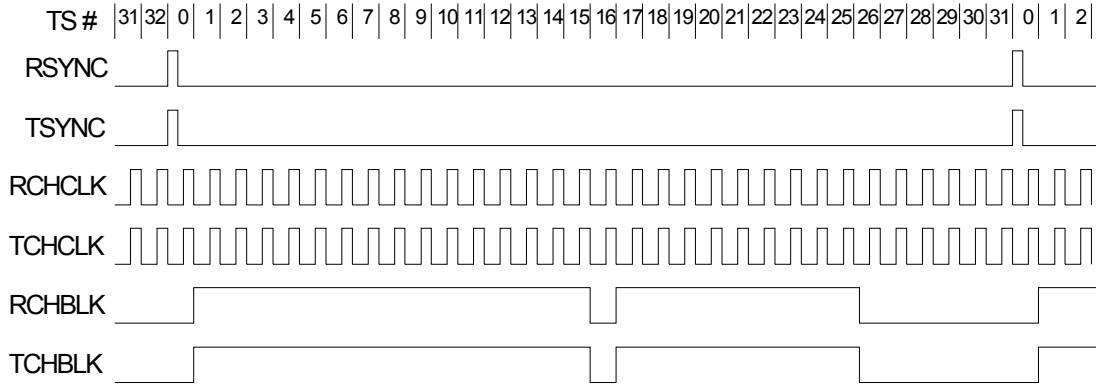


Figure 10-23. E1 G.802 Timing



NOTE: RCHBLK OR TCHBLK PROGRAMMED TO PULSE HIGH DURING TIME SLOTS 1 THROUGH 15, 17 THROUGH 25, AND BIT 1 OF TIME SLOT 26.

11. OPERATING PARAMETERS

ABSOLUTE MAXIMUM RATINGS

| | |
|--|---------------------------------------|
| Voltage Range on Any Lead with Respect to V_{SS} (except V_{DD})..... | -0.3V to +5.5V |
| Supply Voltage (V_{DD}) Range with Respect to V_{SS} | -0.3V to +3.63V |
| Operating Temperature Range | |
| Commercial (DS26524G)..... | 0°C to +70°C |
| Industrial (DS26524GN)..... | -40°C to +85°C (Note 1) |
| Storage Temperature Range..... | -55°C to +125°C |
| Soldering Temperature..... | See IPC/JEDEC J-STD-020 Specification |

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Note 1: Specifications to -40°C are guaranteed by design and not production tested.

Table 11-1. Recommended DC Operating Conditions

($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ for DS26524GN.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------|----------|------------|-------|-----|-------|-------|
| Logic 1 | V_{IH} | | 2.0 | | 5.5 | V |
| Logic 0 | V_{IL} | | -0.3 | | +0.8 | V |
| Supply | V_{DD} | | 3.135 | 3.3 | 3.465 | V |

Table 11-2. Capacitance

($T_A = +25^\circ\text{C}$)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------|-----------|------------|-----|-----|-----|-------|
| Input Capacitance | C_{IN} | | | 7 | | pF |
| Output Capacitance | C_{OUT} | | | 7 | | pF |

Table 11-3. Recommended DC Operating Conditions

($V_{DD} = 3.135\text{V}$ to 3.465V , $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ for DS26524GN.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------|--------------|--------|-----|-------|---------------|
| Supply Current at 3.3V | I_{DD} | (Notes 2, 3) | | 260 | 450 | mA |
| Input Leakage | I_{IL} | | -10.0 | | +10.0 | μA |
| Pullup Pin Input Leakage | I_{ILP} | (Note 4) | -500.0 | | +10.0 | μA |
| Tri-State Output Leakage | I_{OL} | | -10.0 | | +10.0 | μA |
| Output Voltage ($I_o = -1.6\text{mA}$) | V_{OH} | | 2.4 | | | V |
| Output Voltage ($I_o = +0.4\text{mA}$) | V_{OL} | | | | 0.4 | V |

Note 2: $RCLK1-n = TCLK1-n = 2.048\text{MHz}$.

Note 3: Max power dissipation is measured with both ports transmitting an all-ones data pattern with a transmitter load of 100Ω .

Note 4: Pullup pins include DIGIOEN, \overline{JTRST} , JTMS, and JTDI.

11.1 Thermal Characteristics

Table 11-4. Thermal Characteristics

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|------------|-----|-------|------|-------|
| Ambient Temperature (Note 1) | DS26524G | 0 | | +70 | °C |
| | DS26524GN | -40 | | +85 | |
| Junction Temperature | | | | +125 | °C |
| Theta-JA (θ_{JA}) in Still Air for 256-Pin TE-CSBGA | (Note 2) | | +17.5 | | °C/W |

Note 1: The package is mounted on a four-layer JEDEC standard test board.

Note 2: Theta-JA (θ_{JA}) is the junction-to-ambient thermal resistance, when the package is mounted on a four-layer JEDEC standard test board.

11.2 Line Interface Characteristics

Table 11-5. Transmitter Characteristics

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|--------|-----------------|------|------|------|-------|
| Output Mark Amplitude | V_m | E1 75 Ω | 2.13 | 2.37 | 2.61 | V |
| | | E1 120 Ω | 2.70 | 3.00 | 3.30 | |
| | | T1 100 Ω | 2.40 | 3.00 | 3.60 | |
| | | J1 110 Ω | 2.40 | 3.00 | 3.60 | |
| Output Zero Amplitude | V_s | (Note 1) | -0.3 | | +0.3 | V |
| Transmit Amplitude Variation with Supply | | | -1 | | +1 | % |

Table 11-6. Receiver Characteristics

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------------|--------|------------|-----|------|-----|-------|
| Cable Attenuation | Attn | | | | 43 | dB |
| Allowable Zeros Before Loss (Note 1) | | | | 192 | | |
| | | | | 192 | | |
| | | | | 2048 | | |
| Allowable Ones Before Loss (Note 2) | | | | 24 | | |
| | | | | 192 | | |
| | | | | 192 | | |

Note 1: 192 zeros for T1 and T1.231 Specification Compliance. 192 zeros for E1 and G.775 Specification Compliance. 2048 zeros for ETS 300 233 compliance.

Note 2: 24 ones in 192-bit period for T1.231; 192 ones for G.775; 192 ones for ETS 300 233.

12. AC TIMING CHARACTERISTICS

Unless otherwise noted, all timing numbers assume 20pF test load on output signals, 40pF test load on bus signals.

12.1 Microprocessor Bus AC Characteristics

Table 12-1. AC Characteristics—Microprocessor Bus Timing

($V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$ for DS26524GN.) (Note 1) (See [Figure 12-1](#), [Figure 12-2](#), [Figure 12-3](#), and [Figure 12-4](#).)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|--------|------------|-----|-----|-----|-------|
| Setup Time for A[12:0] Valid to \overline{CSB} Active | t1 | | 0 | | | ns |
| Setup Time for \overline{CSB} Active to Either \overline{RDB} , or \overline{WRB} Active | t2 | | 0 | | | ns |
| Delay Time from Either \overline{RDB} or \overline{DSB} Active to D[7:0] Valid | t3 | (Note 2) | | | 125 | ns |
| Hold Time from Either \overline{RDB} or \overline{WRB} Inactive to \overline{CSB} Inactive | t4 | | 0 | | | ns |
| Hold Time from \overline{CSB} or \overline{RDB} or \overline{DSB} Inactive to D[7:0] Tri-State | t5 | | 5 | | 20 | ns |
| Wait Time from \overline{WRB} Active to Latch Data | t6 | | 40 | | | ns |
| Data Setup Time to \overline{WRB} Inactive | t7 | | 10 | | | ns |
| Data Hold Time from \overline{WRB} Inactive | t8 | | 2 | | | ns |
| Address Hold from \overline{WRB} Inactive | t9 | | 0 | | | ns |
| Write Access to Subsequent Write/Read Access Delay Time | t10 | (Note 2) | 80 | | | ns |

Note 1: The timing parameters in this table are guaranteed by design (GBD).

Note 2: If supplying a 1.544MHz MCLK, the FREQSEL bit must be set to meet this timing.

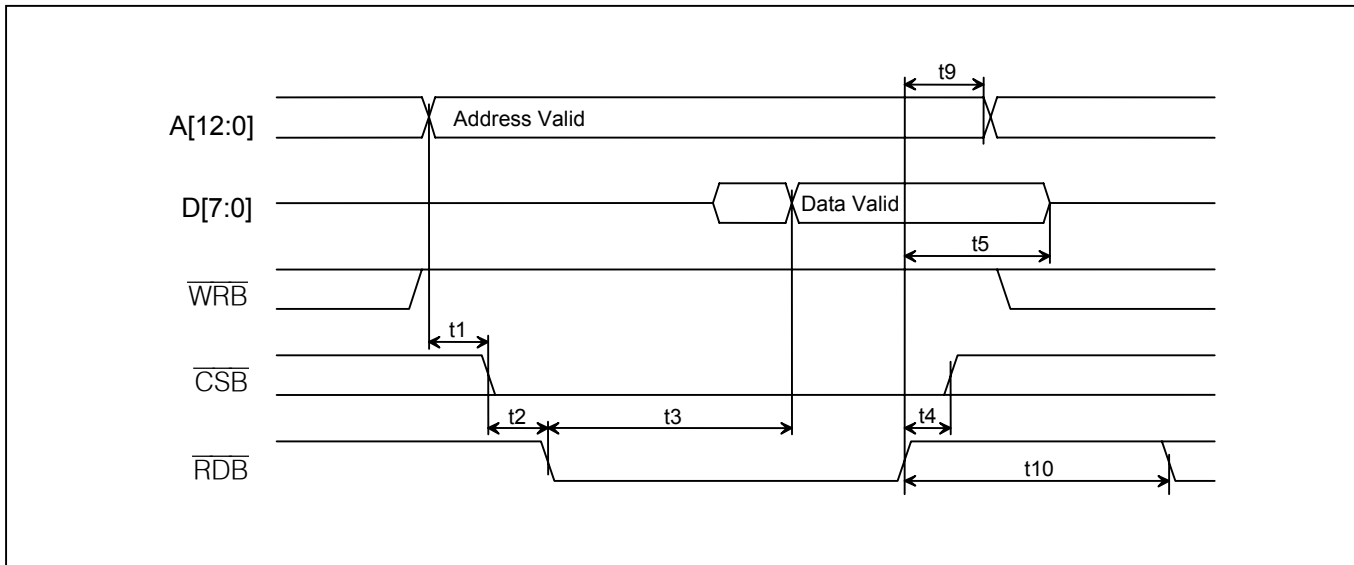
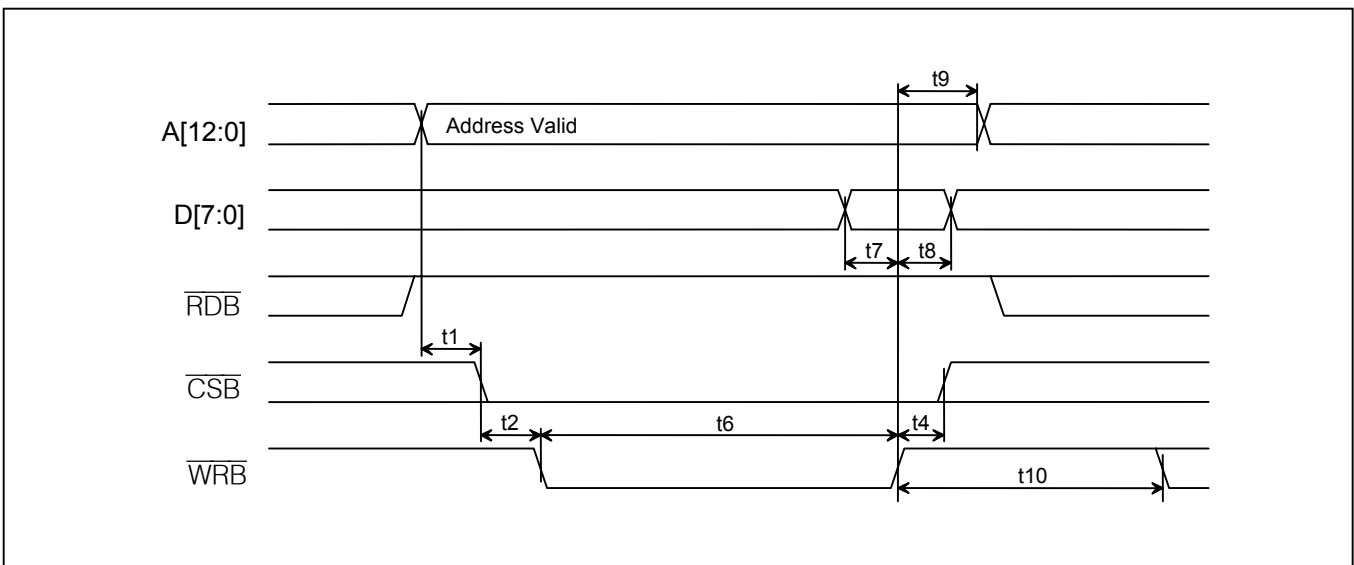
Figure 12-1. Intel Bus Read Timing (BTS = 0)**Figure 12-2. Intel Bus Write Timing (BTS = 0)**

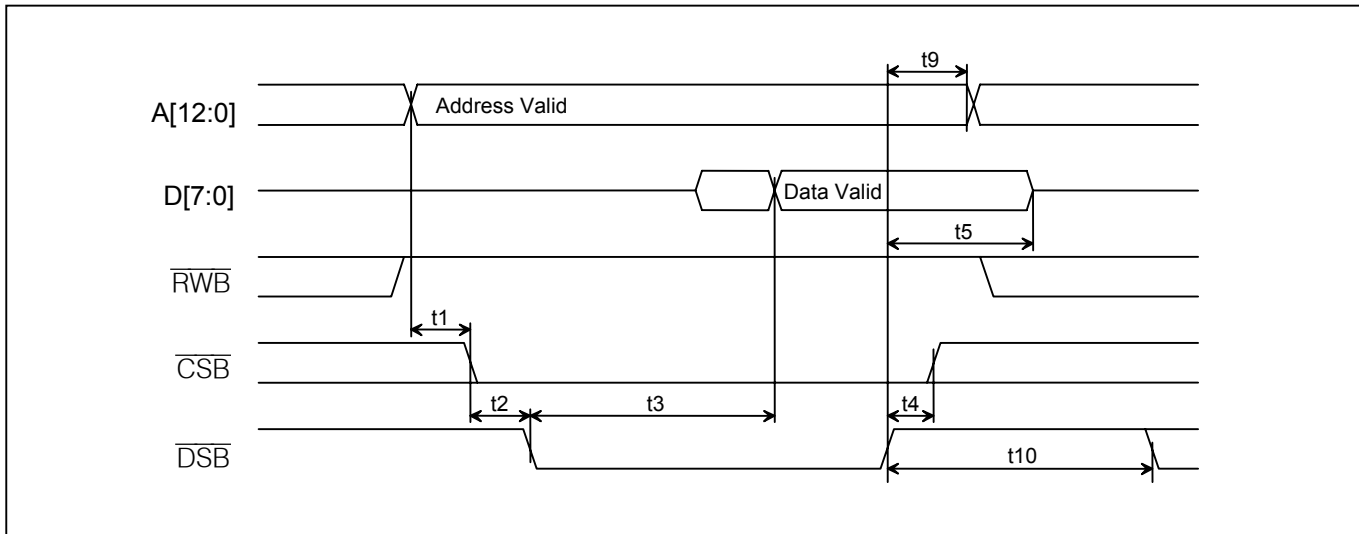
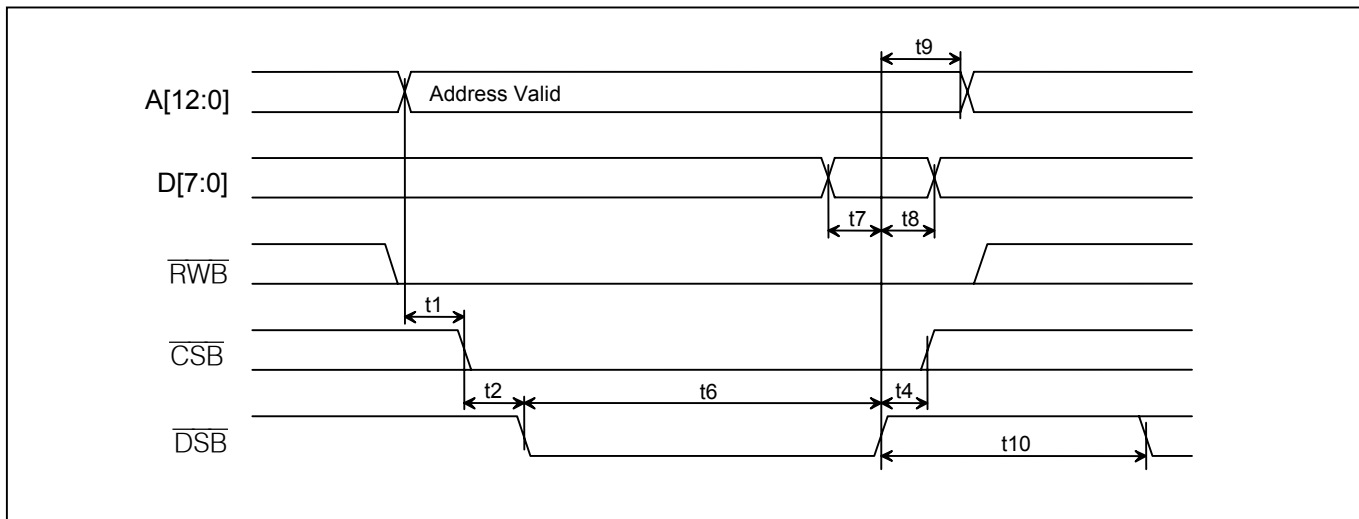
Figure 12-3. Motorola Bus Read Timing (BTS = 1)**Figure 12-4. Motorola Bus Write Timing (BTS = 1)**

Table 12-2. Receiver AC Characteristics

($V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$ for DS26524GN.) (Note 1) (See [Figure 12-5](#), [Figure 12-6](#), and [Figure 12-7](#).)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|----------|------------|-----|-----|--------------|-------|
| RCLK Period | t_{CP} | (Note 2) | | 648 | | ns |
| | | (Note 3) | | 488 | | |
| RCLK Pulse Width | t_{CH} | | 125 | | | ns |
| | t_{CL} | | 125 | | | |
| RSYSCLK Period | t_{SP} | (Note 4) | 60 | 648 | | ns |
| | | (Note 5) | 60 | 488 | | |
| RSYSCLK Pulse Width | t_{SH} | | 30 | | | ns |
| | t_{SL} | | 30 | | | |
| RSYNC Setup to RSYSCLK Falling | t_{SU} | | 20 | | $t_{SH} - 5$ | ns |
| RSYNC Pulse Width | t_{PW} | | 50 | | | ns |
| Delay RCLK to RSER, RSIG Valid | t_{D1} | | | | 50 | ns |
| Delay RCLK to RCHCLK, RSYNC, RCHBLK, RFSYNC | t_{D2} | | | | 50 | ns |
| Delay RSYSCLK to RSER, RSIG Valid | t_{D3} | | | | 50 | ns |
| Delay RSYSCLK to RCHCLK, RCHBLK, RMSYNC, RSYNC | t_{D4} | | | | 50 | ns |

Note 1: The timing parameters in this table are guaranteed by design (GBD).

Note 2: T1 Mode.

Note 3: E1 Mode.

Note 4: RSYSCLK = 1.544MHz.

Note 5: RSYSCLK = 2.048MHz.

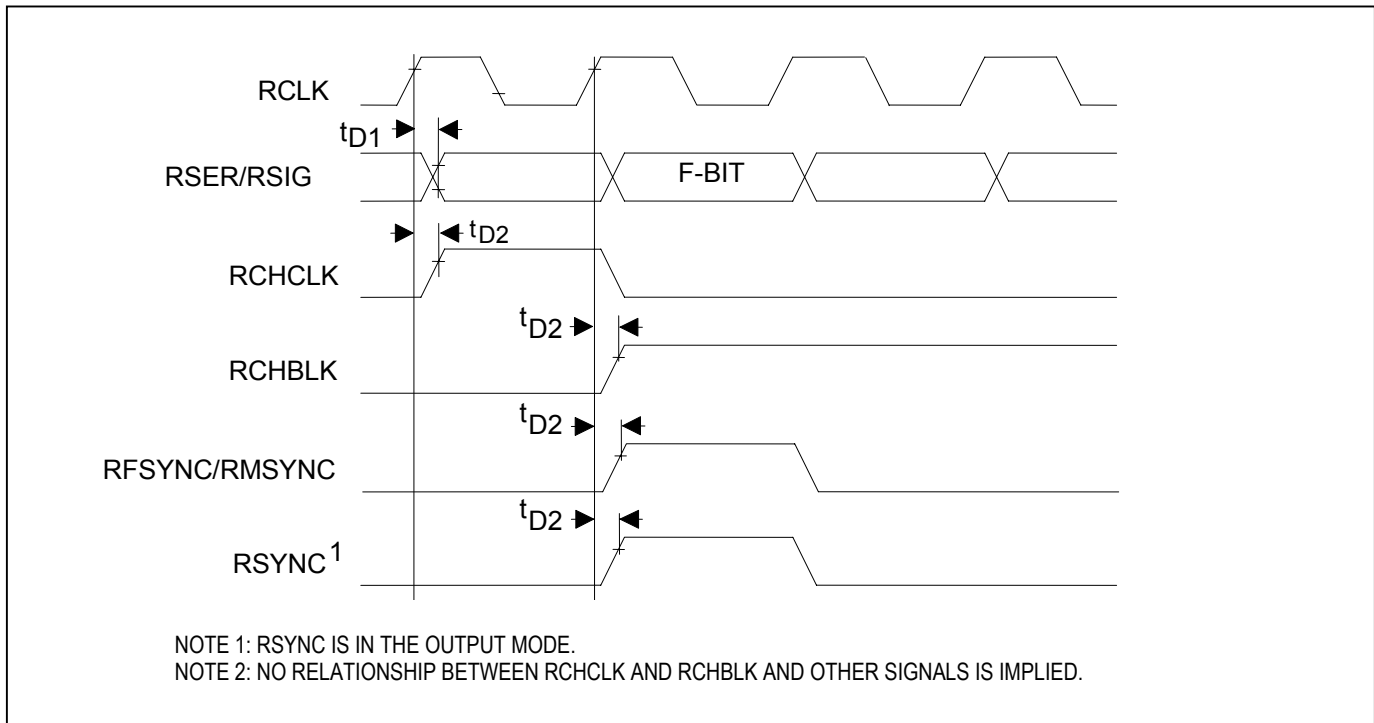
Figure 12-5. Receive Framer Timing—Backplane (T1 Mode)

Figure 12-6. Receive-Side Timing, Elastic Store Enabled (T1 Mode)

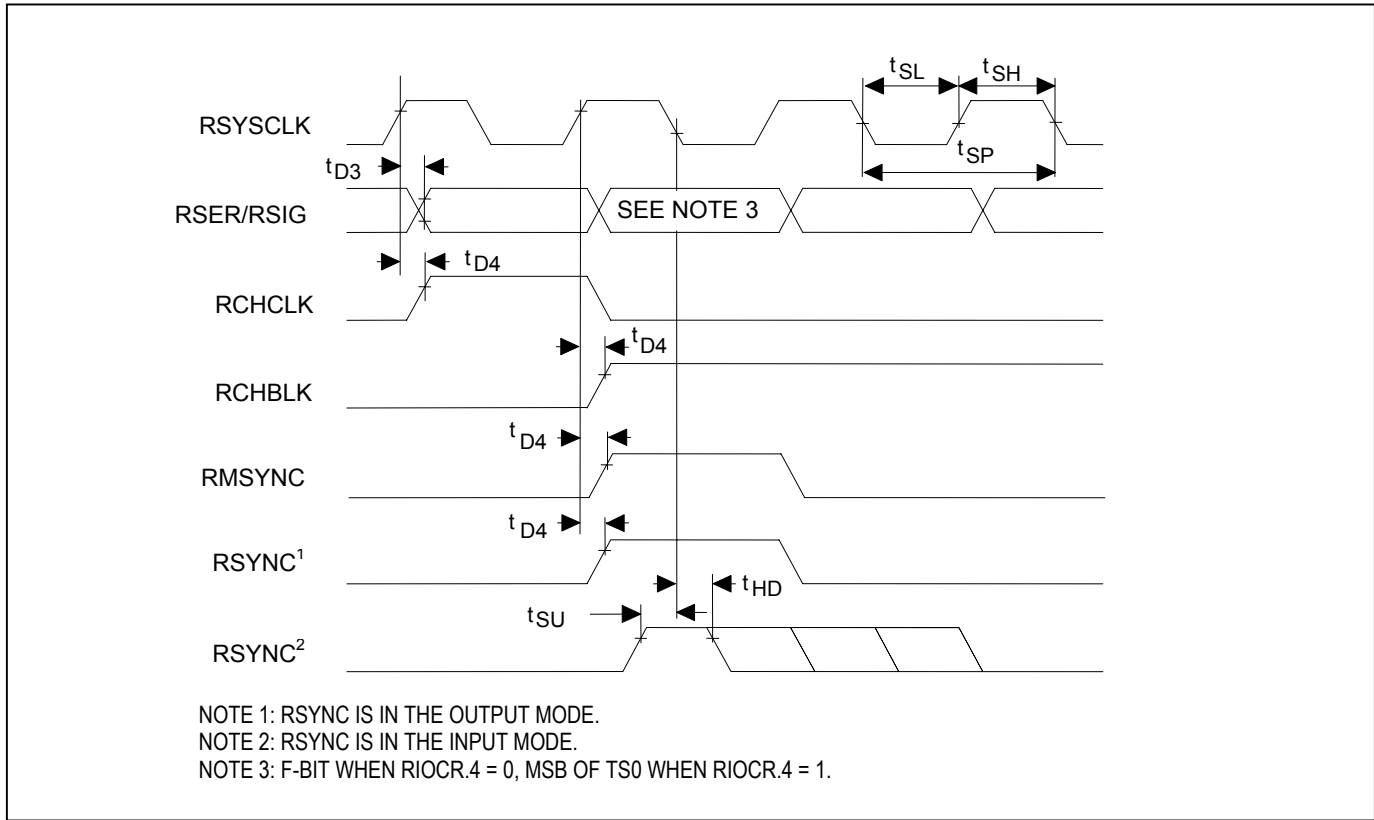


Figure 12-7. Receive Framing Timing—Line Side

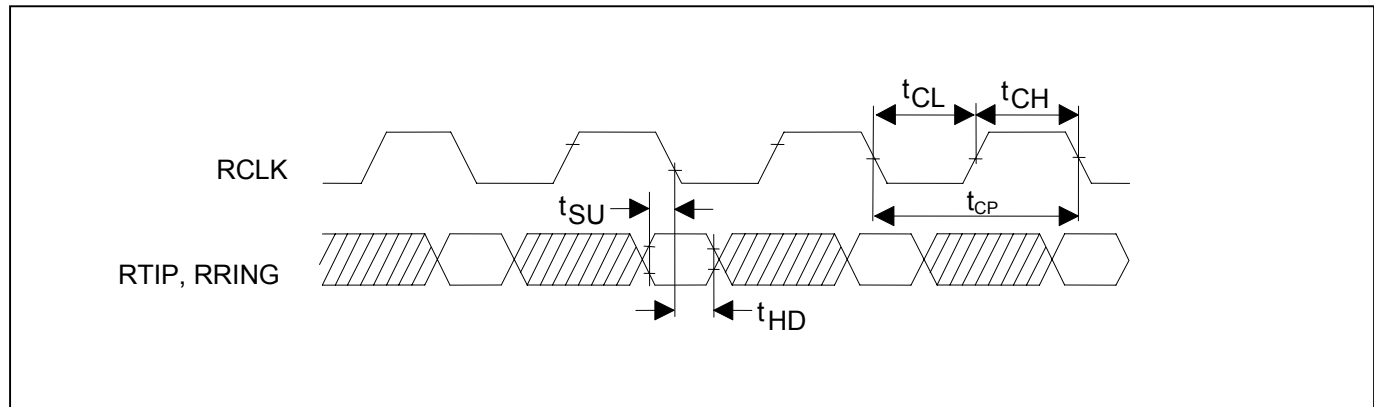


Table 12-3. Transmit AC Characteristics

($V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$ for DS26524GN.) (Note 1) (See [Figure 12-8](#), [Figure 12-9](#), [Figure 12-10](#), and [Figure 12-11](#).)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|----------|------------|-----|-----|------------------------------------|-------|
| TCLK Period | t_{CP} | (Note 2) | | 648 | | ns |
| | | (Note 3) | | 488 | | |
| TCLK Pulse Width | t_{CH} | | 125 | | | ns |
| | t_{CL} | | 125 | | | |
| TSYSCLK Period | t_{SP} | (Note 4) | 60 | 648 | | ns |
| | | (Note 5) | 60 | 448 | | |
| TSYSCLK Pulse Width | t_{SH} | | 30 | | | ns |
| | t_{SL} | | 30 | | | |
| TSYNC or TSSYNCIO Setup to TCLK or TSYSCLK falling | t_{SU} | | 20 | | $t_{CH} - 5$ or $t_{SH} - 5$ | ns |
| TSYNC or TSSYNCIO Pulse Width | t_{PW} | (Note 6) | 50 | | | ns |
| TSSYNCIO Pulse Width (Notes 7, 8) | t_{PW} | | 488 | | | ns |
| | | | 244 | | | |
| | | | 122 | | | |
| | | | 61 | | | |
| TSER, TSIG Setup to TCLK, TSYSCLK Falling | t_{SU} | | 20 | | | ns |
| TSER, TSIG Hold from TCLK, TSYSCLK Falling | t_{HD} | | 20 | | | ns |
| Delay TCLK to TCHBLK, TCHCLK, TSYNC | t_{D2} | | | | 50 | ns |
| Delay TSYSCLK to TCHCLK, TCHBLK | t_{D3} | | | | 50 | ns |
| Delay BPCLK to TSSYNCIO (Note 7) | t_{D5} | | | | 5 | ns |

Note 1: The timing parameters in this table are guaranteed by design (GBD).

Note 2: T1 Mode.

Note 3: E1 Mode.

Note 4: RSYSCLK = 1.544MHz.

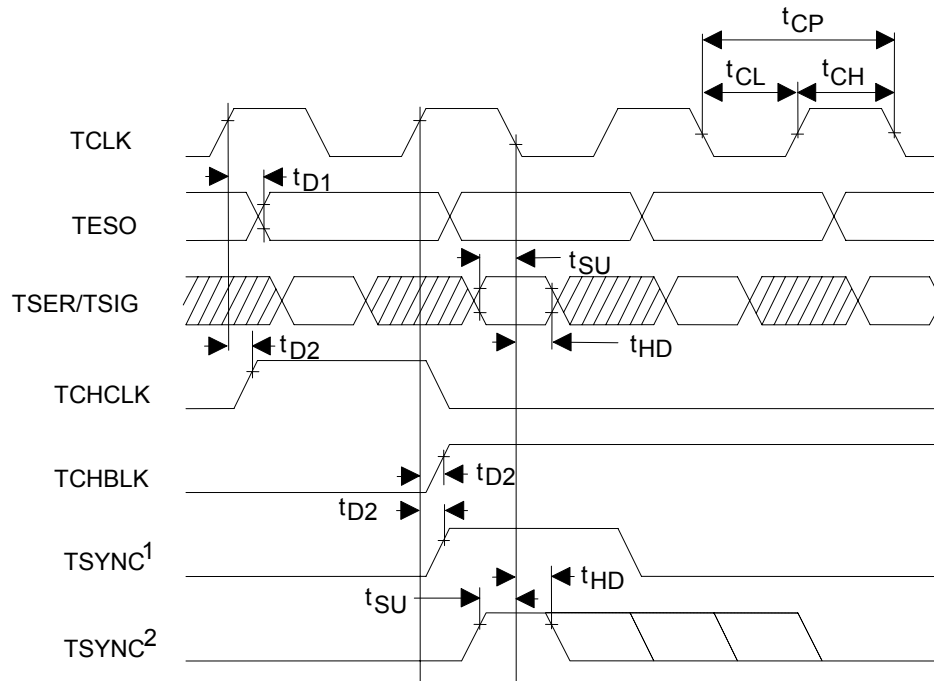
Note 5: RSYSCLK = 2.048MHz.

Note 6: TSSYNCIO configured as an input ([GTCR2.1](#) = 0).

Note 7: TSSYNCIO configured as an output ([GTCR2.1](#) = 1).

Note 8: Varies depending on the frequency of BPCLK.

Figure 12-8. Transmit Formatter Timing—Backplane



NOTE 1: TSYNC IS IN THE OUTPUT MODE.

NOTE 2: TSYNC IS IN THE INPUT MODE.

NOTE 3: TSER IS SAMPLED ON THE FALLING EDGE OF TCLK WHEN THE TRANSMIT-SIDE ELASTIC STORE IS DISABLED.

NOTE 4: TCHCLK AND TCHBLK ARE SYNCHRONOUS WITH TCLK WHEN THE TRANSMIT-SIDE ELASTIC STORE IS DISABLED.

NOTE 5: NO RELATIONSHIP BETWEEN TCHCLK AND TCHBLK AND THE OTHER SIGNALS IS IMPLIED.

Figure 12-9. Transmit Formatter Timing, Elastic Store Enabled

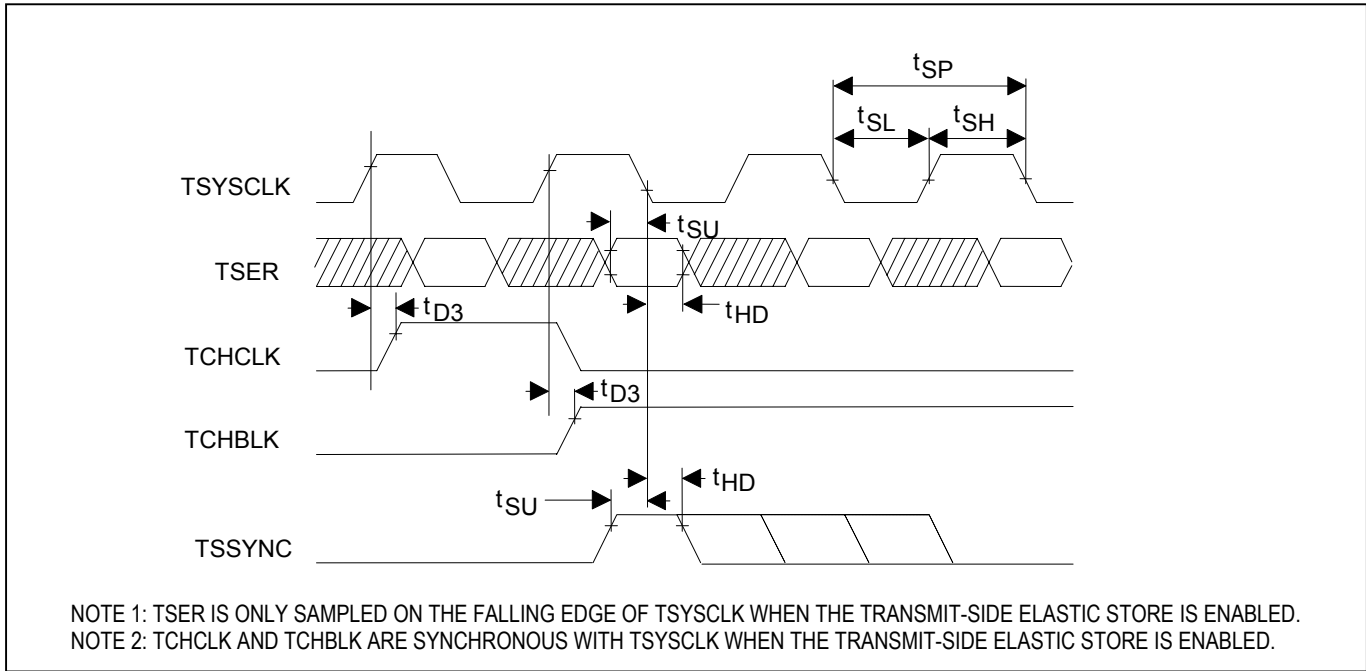


Figure 12-10. BPCLK Timing

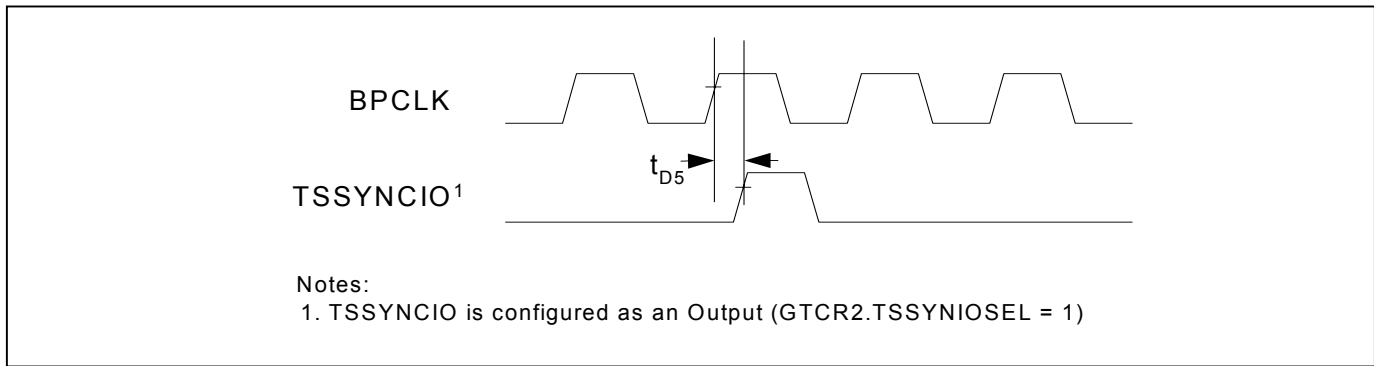
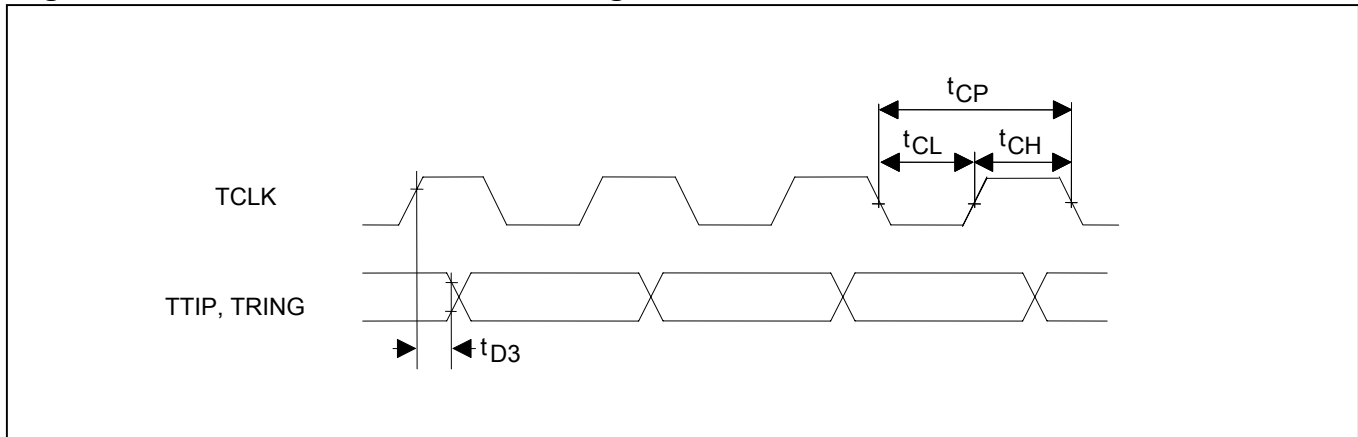


Figure 12-11. Transmit Formatter Timing—Line Side



12.2 JTAG Interface Timing

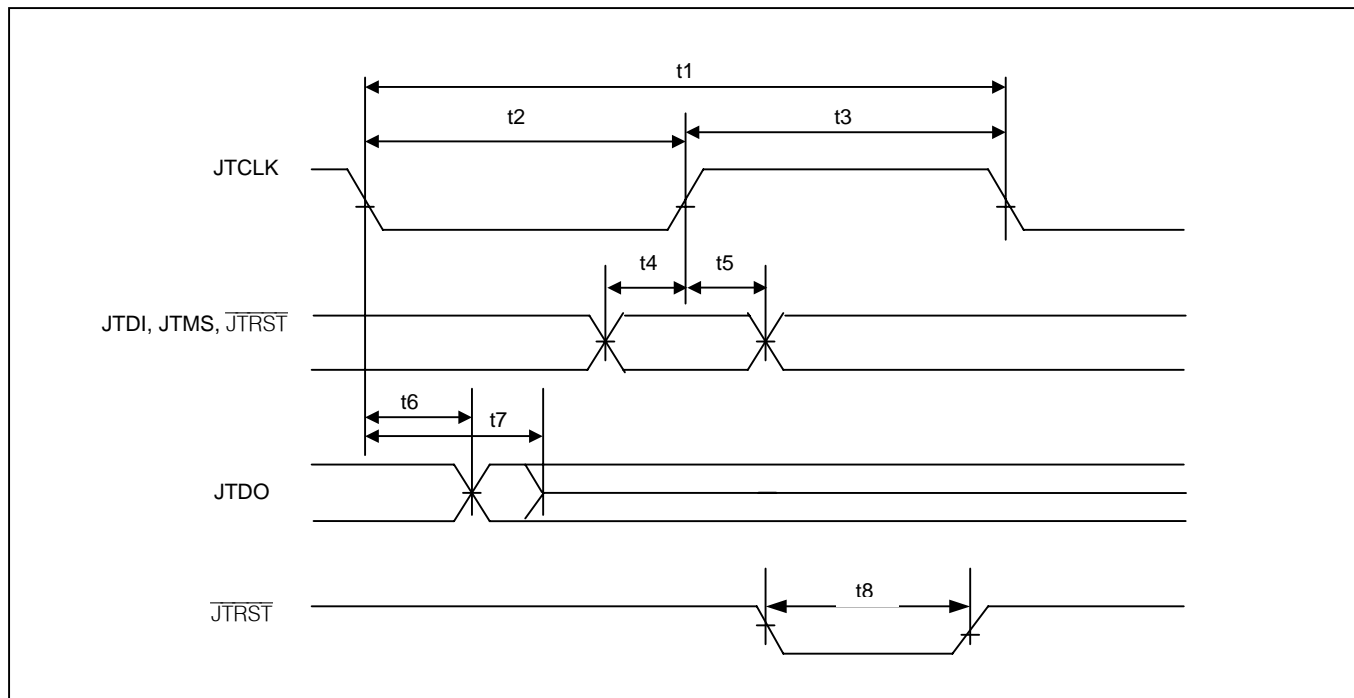
Table 12-4. JTAG Interface Timing

($V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ for DS26524GN.) (See [Figure 12-12.](#))

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|--------|------------|-----|------|-----|-------|
| JTCLK Clock Period | t1 | | | 1000 | | ns |
| JTCLK Clock High:Low Time | t2:t3 | (Note 1) | 50 | 500 | | ns |
| JTCLK to JTDI, JTMS Setup Time | t4 | | 5 | | | ns |
| JTCLK to JTDI, JTMS Hold Time | t5 | | 2 | | | ns |
| JTCLK to JTDO Delay | t6 | | 2 | | 50 | ns |
| JTCLK to JTDO High-Impedance Delay | t7 | | 2 | | 50 | ns |
| $\overline{\text{JTRST}}$ Width Low Time | t8 | | 100 | | | ns |

Note 1: Clock can be stopped high or low.

Figure 12-12. JTAG Interface Timing Diagram



12.3 System Clock AC Characteristics

Table 12-5. System Clock AC Characteristics

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------|--------|------------|-------|-----|-----|-------|
| REF_CLK Frequency | | | 1.544 | | | MHz |
| | | | 2.048 | | | |
| REF_CLK Duty Cycle | | | 40 | | 60 | % |
| Gapped Clock Frequency | | (Note 1) | 43 | 45 | 60 | MHz |
| Gapped Clock Duty Cycle | | | 40 | | 60 | % |

Note 1: The gapped clock is output on the RCHCLK pin when [RESCR](#).6 = 1.

13. JTAG BOUNDARY SCAN AND TEST ACCESS PORT

The DS26524 IEEE 1149.1 design supports the standard instruction codes SAMPLE:PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP, and IDCODE. See [Table 13-1](#). The DS26524 contains the following as required by IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture.

Test Access Port (TAP)

TAP Controller

Instruction Register

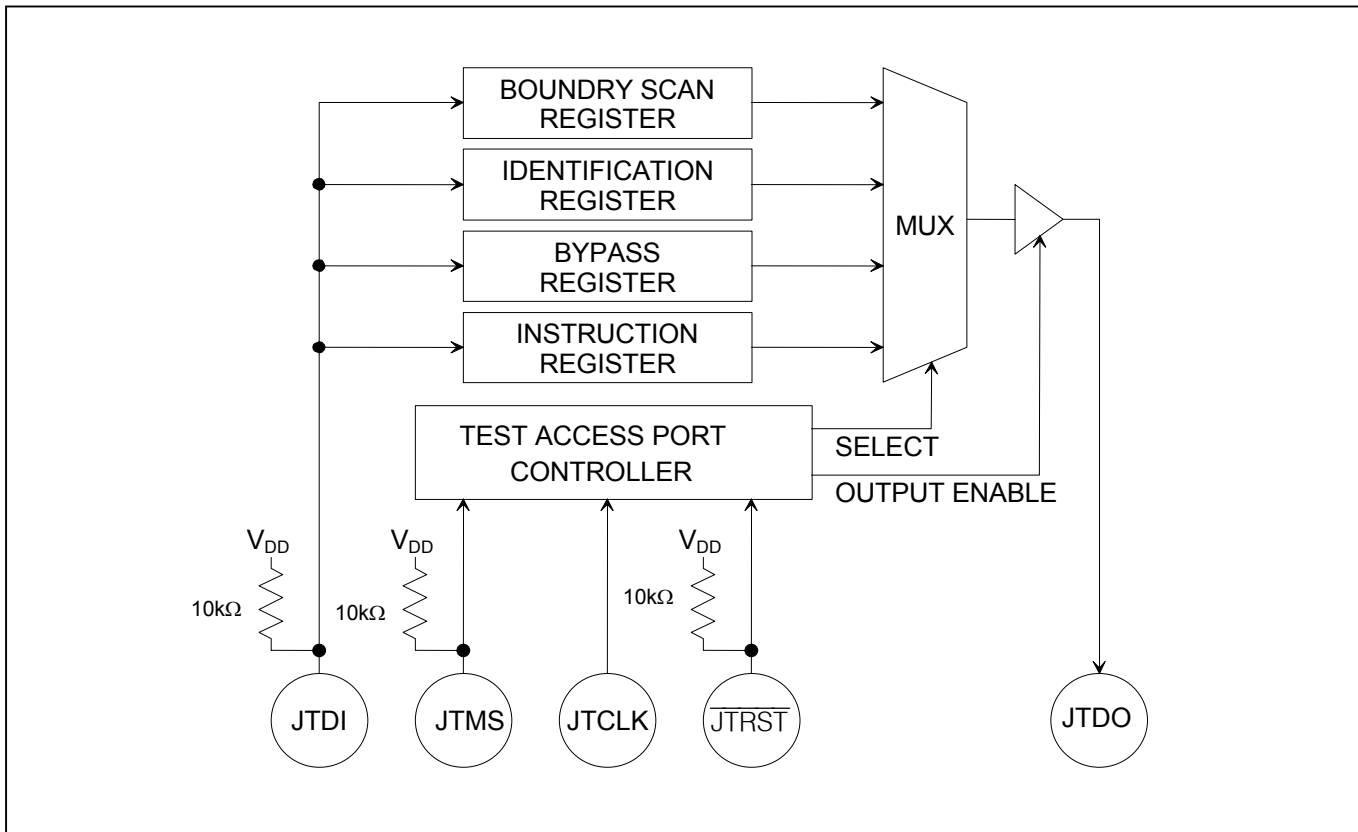
Bypass Register

Boundary Scan Register

Device Identification Register

The Test Access Port has the necessary interface pins: $\overline{\text{JTRST}}$, JTCLK, JTMS, JTDI, and JTDO. See the pin descriptions for details.

Figure 13-1. JTAG Functional Block Diagram



13.1 TAP Controller State Machine

The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK. See [Figure 13-2](#).

13.1.1 Test-Logic-Reset

Upon power-up, the TAP controller is in the Test-Logic-Reset state. The instruction register contains the IDCODE instruction. All system logic of the device operates normally.

13.1.2 Run-Test-Idle

The Run-Test-Idle is used between scan operations or during specific tests. The instruction register and test registers remain idle.

13.1.3 Select-DR-Scan

All test registers retain their previous state. With JTMS LOW, a rising edge of JTCLK moves the controller into the Capture-DR state and initiates a scan sequence. JTMS HIGH during a rising edge on JTCLK moves the controller to the Select-IR-Scan state.

13.1.4 Capture-DR

Data can be parallel-loaded into the test data registers selected by the current instruction. If the instruction does not call for a parallel load or the selected register does not allow parallel loads, the test register remains at its current value. On the rising edge of JTCLK, the controller goes to the Shift-DR state if JTMS is LOW, or it goes to the Exit1-DR state if JTMS is HIGH.

13.1.5 Shift-DR

The test data register selected by the current instruction is connected between JTDI and JTDO and shifts data one stage towards its serial output on each rising edge of JTCLK. If a test register selected by the current instruction is not placed in the serial path, it maintains its previous state.

13.1.6 Exit1-DR

While in this state, a rising edge on JTCLK puts the controller in the Update-DR state, which terminates the scanning process, if JTMS is HIGH. A rising edge on JTCLK with JTMS LOW puts the controller in the Pause-DR state.

13.1.7 Pause-DR

Shifting of the test registers is halted while in this state. All test registers selected by the current instruction retain their previous state. The controller remains in this state while JTMS is LOW. A rising edge on JTCLK with JTMS HIGH puts the controller in the Exit2-DR state.

13.1.8 Exit2-DR

A rising edge on JTCLK with JTMS HIGH while in this state puts the controller in the Update-DR state and terminates the scanning process. A rising edge on JTCLK with JTMS LOW enters the Shift-DR state.

13.1.9 Update-DR

A falling edge on JTCLK while in the Update-DR state latches the data from the shift register path of the test registers into the data output latches. This prevents changes at the parallel output due to changes in the shift register.

13.1.10 Select-IR-Scan

All test registers retain their previous state. The instruction register remains unchanged during this state. With JTMS LOW, a rising edge on JTCLK moves the controller into the Capture-IR state and initiates a scan sequence for the instruction register. JTMS HIGH during a rising edge on JTCLK puts the controller back into the Test-Logic-Reset state.

13.1.11 Capture-IR

The Capture-IR state is used to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of JTCLK. If JTMS is HIGH on the rising edge of JTCLK, the controller enters the Exit1-IR state. If JTMS is LOW on the rising edge of JTCLK, the controller enters the Shift-IR state.

13.1.12 Shift-IR

In this state, the shift register in the instruction register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK towards the serial output. The parallel register, as well as all test registers, remains at their previous states. A rising edge on JTCLK with JTMS HIGH moves the controller to the Exit1-IR state. A rising edge on JTCLK with JTMS LOW keeps the controller in the Shift-IR state while moving data one stage through the instruction shift register.

13.1.13 Exit1-IR

A rising edge on JTCLK with JTMS LOW puts the controller in the Pause-IR state. If JTMS is HIGH on the rising edge of JTCLK, the controller enters the Update-IR state and terminates the scanning process.

13.1.14 Pause-IR

Shifting of the instruction shift register is halted temporarily. With JTMS HIGH, a rising edge on JTCLK puts the controller in the Exit2-IR state. The controller remains in the Pause-IR state if JTMS is LOW during a rising edge on JTCLK.

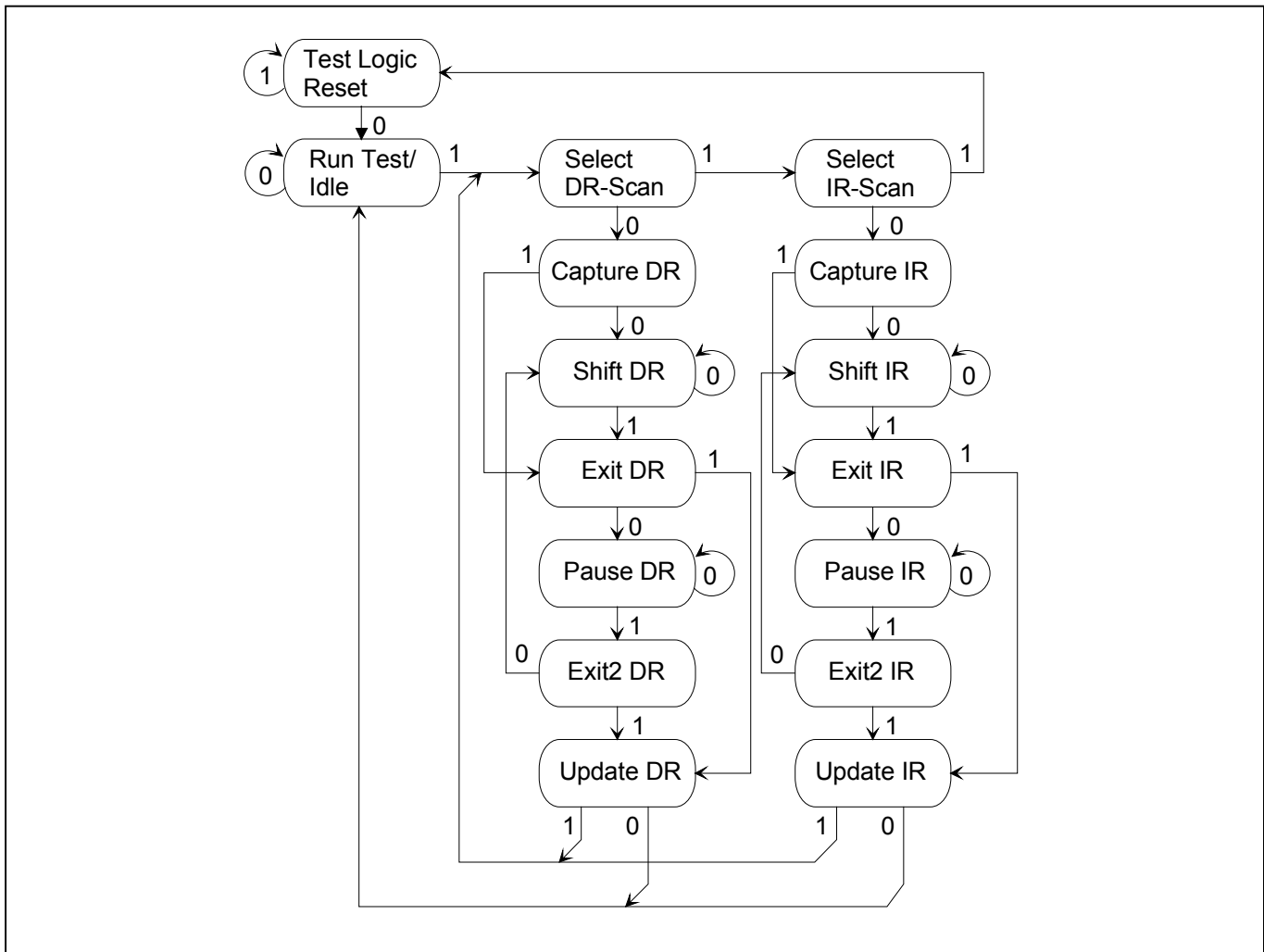
13.1.15 Exit2-IR

A rising edge on JTCLK with JTMS LOW puts the controller in the Update-IR state. The controller loops back to Shift-IR if JTMS is HIGH during a rising edge of JTCLK in this state.

13.1.16 Update-IR

The instruction code shifted into the instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS LOW puts the controller in the Run-Test-Idle state. With JTMS HIGH, the controller enters the Select-DR-Scan state.

Figure 13-2. TAP Controller State Diagram



13.2 Instruction Register

The instruction register contains a shift register as well as a latched parallel output, and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register will be connected between JTDI and JTDO. While in the Shift-IR state, a rising edge on JTCLK with JTMS LOW will shift the data one stage towards the serial output at JTDO. A rising edge on JTCLK in the Exit1-IR state or the Exit2-IR state with JTMS HIGH will move the controller to the Update-IR state. The falling edge of that same JTCLK will latch the data in the instruction shift register to the instruction parallel output. Instructions supported by the DS26524 and its respective operational binary codes are shown in [Table 13-1](#).

Table 13-1. Instruction Codes for IEEE 1149.1 Architecture

| INSTRUCTION | SELECTED REGISTER | INSTRUCTION CODES |
|----------------|-----------------------|-------------------|
| SAMPLE:PRELOAD | Boundary Scan | 010 |
| BYPASS | Bypass | 111 |
| EXTEST | Boundary Scan | 000 |
| CLAMP | Bypass | 011 |
| HIGHZ | Bypass | 100 |
| IDCODE | Device Identification | 001 |

13.2.1 SAMPLE:PRELOAD

This is a mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. The digital I/Os of the device can be sampled at the boundary scan register without interfering with the normal operation of the device by using the Capture-DR state. SAMPLE:PRELOAD also allows the device to shift data into the boundary scan register via JTDI using the Shift-DR state.

13.2.2 BYPASS

When the BYPASS instruction is latched into the parallel instruction register, JTDI connects to JTDO through the one-bit bypass test register. This allows data to pass from JTDI to JTDO without affecting the device's normal operation.

13.2.3 EXTEST

This allows testing of all interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur. Once enabled via the Update-IR state, the parallel outputs of all digital output pins will be driven. The boundary scan register will be connected between JTDI and JTDO. The Capture-DR will sample all digital inputs into the boundary scan register.

13.2.4 CLAMP

All digital outputs of the device will output data from the boundary scan parallel output while connecting the bypass register between JTDI and JTDO. The outputs will not change during the CLAMP instruction.

13.2.5 HIGHZ

All digital outputs of the device will be placed in a high-impedance state. The BYPASS register will be connected between JTDI and JTDO.

13.2.6 IDCODE

When the IDCODE instruction is latched into the parallel instruction register, the identification test register is selected. The device identification code will be loaded into the identification register on the rising edge of JTCLK following entry into the Capture-DR state. Shift-DR can be used to shift the identification code out serially via JTDO. During Test-Logic-Reset, the identification code is forced into the instruction register's parallel output. The ID code will always have a 1 in the LSB position. The next 11 bits identify the manufacturer's JEDEC number and number of continuation bytes followed by 16 bits for the device and 4 bits for the version.

13.3 JTAG ID Codes

Table 13-2. ID Code Structure

| DEVICE | REVISION ID[31:28] | DEVICE CODE ID[27:12] | MANUFACTURER'S CODE ID[11:1] | REQUIRED ID[0] |
|---------|--------------------|-----------------------|------------------------------|----------------|
| DS26528 | Consult factory | 0000000000110111 | 00010100001 | 1 |
| DS26524 | Consult factory | 0000000000111001 | 00010100001 | 1 |

13.4 Test Registers

IEEE 1149.1 requires a minimum of two test registers: the bypass register and the boundary scan register. An optional test register has been included with the DS26524 design. This test register is the identification register and is used in conjunction with the IDCODE instruction and the Test-Logic-Reset state of the TAP controller.

13.4.1 Boundary Scan Register

This register contains both a shift register path and a latched parallel output for all control cells and digital I/O cells, and is n bits in length. See [Table 13-3](#) for all the cell bit locations and definitions.

13.4.2 Bypass Register

This is a single one-bit shift register used in conjunction with the BYPASS, CLAMP, and HIGHZ instructions, which provides a short path between JTDI and JTDO.

13.4.3 Identification Register

The identification register contains a 32-bit shift register and a 32-bit latched parallel output. This register is selected during the IDCODE instruction and when the TAP controller is in the Test-Logic-Reset state.

Table 13-3. Boundary Scan Control Bits

| CELL# | NAME | TYPE | CONTROL CELL |
|-------|---------------|--------------|--------------|
| 0 | — | controlr | |
| 1 | rser(1) | output3 | 0 |
| 2 | — | controlr | |
| 3 | rm_rfsync(1) | output3 | 2 |
| 4 | rm_rfsync(1) | observe_only | |
| 5 | — | controlr | |
| 6 | rsync(1) | output3 | 5 |
| 7 | rsync(1) | observe_only | |
| 8 | — | controlr | |
| 9 | tsig(1) | output3 | 8 |
| 10 | tsig(1) | observe_only | |
| 11 | — | controlr | |
| 12 | tsync(1) | output3 | 11 |
| 13 | tsync(1) | observe_only | |
| 14 | tser(1) | observe_only | |
| 15 | tclk(1) | observe_only | |
| 16 | — | controlr | |
| 17 | tchblk_clk(1) | output3 | 16 |
| 18 | tchblk_clk(1) | observe_only | |
| 19 | — | controlr | |

| CELL# | NAME | TYPE | CONTROL CELL |
|-------|-----------------|--------------|--------------|
| 20 | rchblk_clk(2) | output3 | 19 |
| 21 | rchblk_clk(2) | observe_only | |
| 22 | — | controlr | |
| 23 | rsg(2) | output3 | 22 |
| 24 | rsg(2) | observe_only | |
| 25 | — | controlr | |
| 26 | rfl_ttc(2) | output3 | 25 |
| 27 | — | controlr | |
| 28 | al_rsig_flos(2) | output3 | 27 |
| 29 | — | controlr | |
| 30 | rser(2) | output3 | 29 |
| 31 | — | controlr | |
| 32 | rm_rfsync(2) | output3 | 31 |
| 33 | rm_rfsync(2) | observe_only | |
| 34 | — | controlr | |
| 35 | rsync(2) | output3 | 34 |
| 36 | rsync(2) | observe_only | |
| 37 | — | controlr | |
| 38 | tsig(2) | output3 | 37 |
| 39 | tsig(2) | observe_only | |

| CELL# | NAME | TYPE | CONTROL CELL |
|-------|---------------|--------------|--------------|
| 40 | — | controlr | |
| 41 | tsync(2) | output3 | 40 |
| 42 | tsync(2) | observe_only | |
| 43 | tser(2) | observe_only | |
| 44 | tclk(2) | observe_only | |
| 45 | — | controlr | |
| 46 | tchblk_clk(2) | output3 | 45 |
| 47 | tchblk_clk(2) | observe_only | |
| 48 | mclk | observe_only | |
| 49 | — | controlr | |
| 50 | refclkio | output3 | 49 |
| 51 | refclkio | observe_only | |
| 52 | — | controlr | |
| 53 | bpclk | output3 | 52 |
| 54 | a(12) | observe_only | |
| 55 | a(11) | observe_only | |
| 56 | a(10) | observe_only | |
| 57 | digio_en | observe_only | |
| 58 | a(9) | observe_only | |
| 59 | a(8) | observe_only | |
| 60 | a(7) | observe_only | |
| 61 | a(6) | observe_only | |
| 62 | a(5) | observe_only | |
| 63 | a(4) | observe_only | |
| 64 | a(3) | observe_only | |
| 65 | a(2) | observe_only | |
| 66 | a(1) | observe_only | |
| 67 | a(0) | observe_only | |
| 68 | — | controlr | |
| 69 | tchblk_clk(7) | output3 | 68 |
| 70 | tchblk_clk(7) | observe_only | |
| 71 | tclk(7) | observe_only | |
| 72 | tser(7) | observe_only | |
| 73 | — | controlr | |
| 74 | tsync(7) | output3 | 73 |
| 75 | tsync(7) | observe_only | |
| 76 | — | controlr | |
| 77 | tsig(7) | output3 | 76 |
| 78 | tsig(7) | observe_only | |
| 79 | — | controlr | |
| 80 | rsync(7) | output3 | 79 |
| 81 | rsync(7) | observe_only | |

| CELL# | NAME | TYPE | CONTROL CELL |
|-------|------------------|--------------|--------------|
| 82 | — | controlr | |
| 83 | rm_rfsync(7) | output3 | 82 |
| 84 | rm_rfsync(7) | observe_only | |
| 85 | — | controlr | |
| 86 | rser(7) | output3 | 85 |
| 87 | — | controlr | |
| 88 | al_rsigf_flos(7) | output3 | 87 |
| 89 | — | controlr | |
| 90 | rfl_ltc(7) | output3 | 89 |
| 91 | — | controlr | |
| 92 | rsig(7) | output3 | 91 |
| 93 | rsig(7) | observe_only | |
| 94 | — | controlr | |
| 95 | rchblk_clk(7) | output3 | 94 |
| 96 | rchblk_clk(7) | observe_only | |
| 97 | — | controlr | |
| 98 | tchblk_clk(8) | output3 | 97 |
| 99 | tchblk_clk(8) | observe_only | |
| 100 | tclk(8) | observe_only | |
| 101 | tser(8) | observe_only | |
| 102 | — | controlr | |
| 103 | tsync(8) | output3 | 102 |
| 104 | tsync(8) | observe_only | |
| 105 | — | controlr | |
| 106 | tsig(8) | output3 | 105 |
| 107 | tsig(8) | observe_only | |
| 108 | — | controlr | |
| 109 | rsync(8) | output3 | 108 |
| 110 | rsync(8) | observe_only | |
| 111 | — | controlr | |
| 112 | rm_rfsync(8) | output3 | 111 |
| 113 | rm_rfsync(8) | observe_only | |
| 114 | — | controlr | |
| 115 | rser(8) | output3 | 114 |
| 116 | — | controlr | |
| 117 | al_rsigf_flos(8) | output3 | 116 |
| 118 | — | controlr | |
| 119 | rfl_ltc(8) | output3 | 118 |
| 120 | — | controlr | |
| 121 | rclk(8) | output3 | 120 |
| 122 | rclk(8) | observe_only | |
| 123 | — | controlr | |

| CELL# | NAME | TYPE | CONTROL CELL |
|-------|------------------|--------------|--------------|
| 124 | rclk(7) | output3 | 123 |
| 125 | rclk(7) | observe_only | |
| 126 | — | controlr | |
| 127 | rsig(8) | output3 | 126 |
| 128 | rsig(8) | observe_only | |
| 129 | — | controlr | |
| 130 | rchblk_clk(8) | output3 | 129 |
| 131 | rchblk_clk(8) | observe_only | |
| 132 | — | controlr | |
| 133 | rclk(6) | output3 | 132 |
| 134 | rclk(6) | observe_only | |
| 135 | — | controlr | |
| 136 | rclk(5) | output3 | 135 |
| 137 | rclk(5) | observe_only | |
| 138 | resetb | observe_only | |
| 139 | txen_b | observe_only | |
| 140 | bts | observe_only | |
| 141 | rsysclk | observe_only | |
| 142 | — | controlr | |
| 143 | tssyncio | output3 | 142 |
| 144 | tssyncio | observe_only | |
| 145 | tsysclk | observe_only | |
| 146 | — | controlr | |
| 147 | rchblk_clk(6) | output3 | 146 |
| 148 | rchblk_clk(6) | observe_only | |
| 149 | — | controlr | |
| 150 | rsig(6) | output3 | 149 |
| 151 | rsig(6) | observe_only | |
| 152 | — | controlr | |
| 153 | rif_ltc(6) | output3 | 152 |
| 154 | — | controlr | |
| 155 | al_rsigf_flos(6) | output3 | 154 |
| 156 | — | controlr | |
| 157 | rser(6) | output3 | 156 |
| 158 | — | controlr | |
| 159 | rm_rfsync(6) | output3 | 158 |
| 160 | rm_rfsync(6) | observe_only | |
| 161 | — | controlr | |
| 162 | rsync(6) | output3 | 161 |
| 163 | rsync(6) | observe_only | |
| 164 | — | controlr | |
| 165 | tsig(6) | output3 | 164 |

| CELL# | NAME | TYPE | CONTROL CELL |
|-------|------------------|--------------|--------------|
| 166 | tsig(6) | observe_only | |
| 167 | — | controlr | |
| 168 | tsync(6) | output3 | 167 |
| 169 | tsync(6) | observe_only | |
| 170 | tser(6) | observe_only | |
| 171 | tclk(6) | observe_only | |
| 172 | — | controlr | |
| 173 | tchblk_clk(6) | output3 | 172 |
| 174 | tchblk_clk(6) | observe_only | |
| 175 | — | controlr | |
| 176 | rchblk_clk(5) | output3 | 175 |
| 177 | rchblk_clk(5) | observe_only | |
| 178 | — | controlr | |
| 179 | rsig(5) | output3 | 178 |
| 180 | rsig(5) | observe_only | |
| 181 | — | controlr | |
| 182 | rif_ltc(5) | output3 | 181 |
| 183 | — | controlr | |
| 184 | al_rsigf_flos(5) | output3 | 183 |
| 185 | — | controlr | |
| 186 | rser(5) | output3 | 185 |
| 187 | — | controlr | |
| 188 | rm_rfsync(5) | output3 | 187 |
| 189 | rm_rfsync(5) | observe_only | |
| 190 | — | controlr | |
| 191 | rsync(5) | output3 | 190 |
| 192 | rsync(5) | observe_only | |
| 193 | — | controlr | |
| 194 | tsig(5) | output3 | 193 |
| 195 | tsig(5) | observe_only | |
| 196 | — | controlr | |
| 197 | tsync(5) | output3 | 196 |
| 198 | tsync(5) | observe_only | |
| 199 | tser(5) | observe_only | |
| 200 | tclk(5) | observe_only | |
| 201 | — | controlr | |
| 202 | tchblk_clk(5) | output3 | 201 |
| 203 | tchblk_clk(5) | observe_only | |
| 204 | — | controlr | |
| 205 | intb | output3 | 204 |
| 206 | d(7) | output3 | 220 |
| 207 | d(7) | observe_only | |

| CELL# | NAME | TYPE | CONTROL CELL |
|-------|------------------|--------------|--------------|
| 208 | d(6) | output3 | 220 |
| 209 | d(6) | observe_only | |
| 210 | d(5) | output3 | 220 |
| 211 | d(5) | observe_only | |
| 212 | d(4) | output3 | 220 |
| 213 | d(4) | observe_only | |
| 214 | d(3) | output3 | 220 |
| 215 | d(3) | observe_only | |
| 216 | d(2) | output3 | 220 |
| 217 | d(2) | observe_only | |
| 218 | d(1) | output3 | 220 |
| 219 | d(1) | observe_only | |
| 220 | — | controlr | |
| 221 | d(0) | output3 | 220 |
| 222 | d(0) | observe_only | |
| 223 | rdb_dsb | observe_only | |
| 224 | wrb_rwb | observe_only | |
| 225 | csb | observe_only | |
| 226 | — | controlr | |
| 227 | tchblk_clk(4) | output3 | 226 |
| 228 | tchblk_clk(4) | observe_only | |
| 229 | tclk(4) | observe_only | |
| 230 | tser(4) | observe_only | |
| 231 | — | controlr | |
| 232 | tsync(4) | output3 | 231 |
| 233 | tsync(4) | observe_only | |
| 234 | — | controlr | |
| 235 | tsig(4) | output3 | 234 |
| 236 | tsig(4) | observe_only | |
| 237 | — | controlr | |
| 238 | rsync(4) | output3 | 237 |
| 239 | rsync(4) | observe_only | |
| 240 | — | controlr | |
| 241 | rm_rfsync(4) | output3 | 240 |
| 242 | rm_rfsync(4) | observe_only | |
| 243 | — | controlr | |
| 244 | rser(4) | output3 | 243 |
| 245 | — | controlr | |
| 246 | al_rsigf_flos(4) | output3 | 245 |
| 247 | — | controlr | |
| 248 | rif_ltc(4) | output3 | 247 |
| 249 | — | controlr | |

| CELL# | NAME | TYPE | CONTROL CELL |
|-------|------------------|--------------|--------------|
| 250 | rsig(4) | output3 | 249 |
| 251 | rsig(4) | observe_only | |
| 252 | — | controlr | |
| 253 | rchblk_clk(4) | output3 | 252 |
| 254 | rchblk_clk(4) | observe_only | |
| 255 | — | controlr | |
| 256 | tchblk_clk(3) | output3 | 255 |
| 257 | tchblk_clk(3) | observe_only | |
| 258 | tclk(3) | observe_only | |
| 259 | tser(3) | observe_only | |
| 260 | — | controlr | |
| 261 | tsync(3) | output3 | 260 |
| 262 | tsync(3) | observe_only | |
| 263 | — | controlr | |
| 264 | tsig(3) | output3 | 263 |
| 265 | tsig(3) | observe_only | |
| 266 | — | controlr | |
| 267 | rsync(3) | output3 | 266 |
| 268 | rsync(3) | observe_only | |
| 269 | — | controlr | |
| 270 | rm_rfsync(3) | output3 | 269 |
| 271 | rm_rfsync(3) | observe_only | |
| 272 | — | controlr | |
| 273 | rser(3) | output3 | 272 |
| 274 | — | controlr | |
| 275 | al_rsigf_flos(3) | output3 | 274 |
| 276 | — | controlr | |
| 277 | rif_ltc(3) | output3 | 276 |
| 278 | — | controlr | |
| 279 | rsig(3) | output3 | 278 |
| 280 | rsig(3) | observe_only | |
| 281 | — | controlr | |
| 282 | rchblk_clk(3) | output3 | 281 |
| 283 | rchblk_clk(3) | observe_only | |
| 284 | — | controlr | |
| 285 | rclk(4) | output3 | 284 |
| 286 | rclk(4) | observe_only | |
| 287 | — | controlr | |
| 288 | rclk(3) | output3 | 287 |
| 289 | rclk(3) | observe_only | |
| 290 | — | controlr | |
| 291 | rclk(2) | output3 | 290 |

| CELL# | NAME | TYPE | CONTROL CELL |
|-------|---------------|--------------|--------------|
| 292 | rclk(2) | observe_only | |
| 293 | — | controlr | |
| 294 | rclk(1) | output3 | 293 |
| 295 | rclk(1) | observe_only | |
| 296 | — | controlr | |
| 297 | rchblk_clk(1) | output3 | 296 |
| 298 | rchblk_clk(1) | observe_only | |

| CELL# | NAME | TYPE | CONTROL CELL |
|-------|------------------|--------------|--------------|
| 299 | — | controlr | |
| 300 | rsig(1) | output3 | 299 |
| 301 | rsig(1) | observe_only | |
| 302 | — | controlr | |
| 303 | r1f_ltc(1) | output3 | 302 |
| 304 | — | controlr | |
| 305 | al_rsigf_flos(1) | output3 | 304 |

14. PIN CONFIGURATION

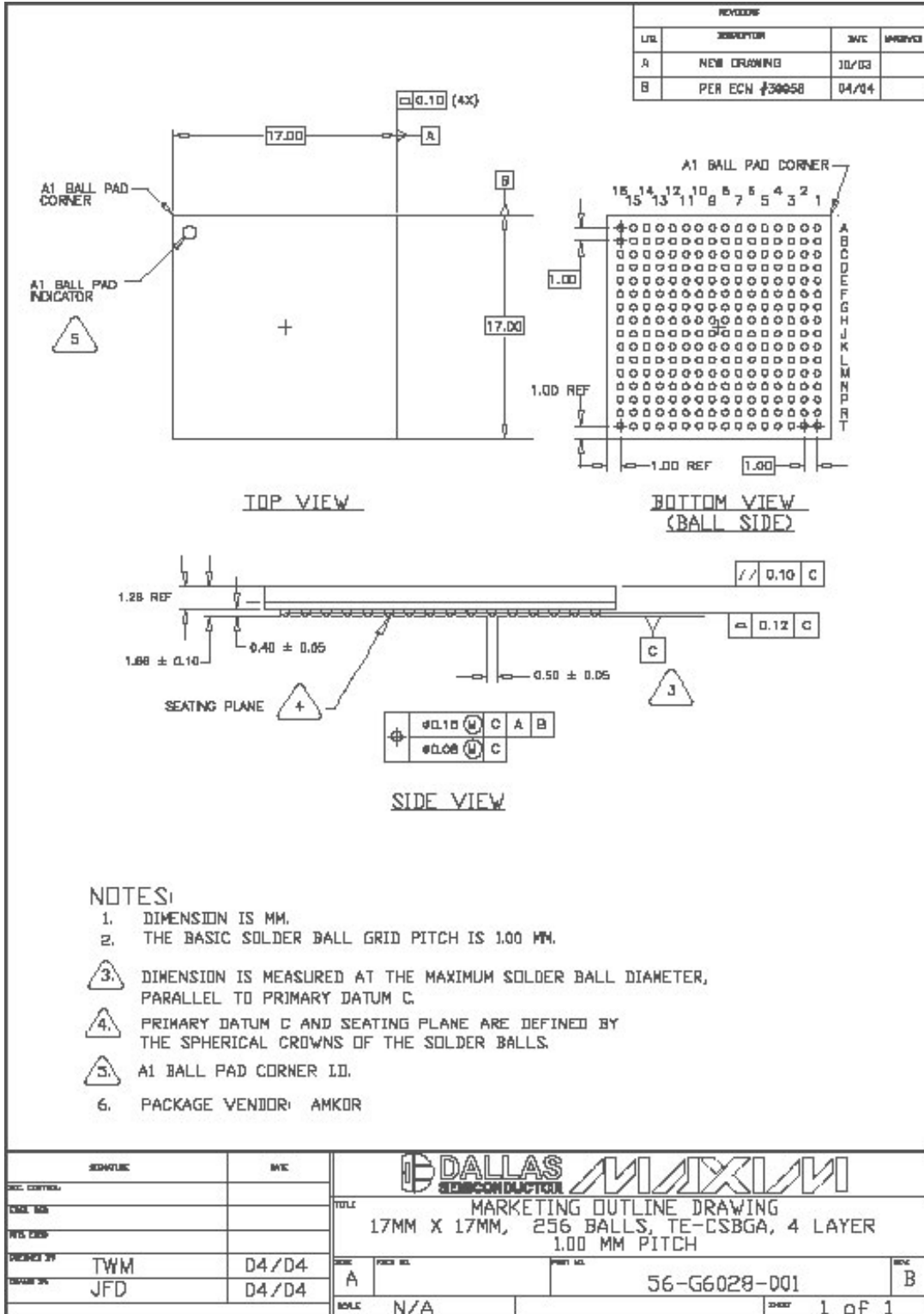
Figure 14-1. Pin Configuration—256-Ball TE-CSBGA

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
|----------|--------|--------|-----------------------|---------------------|---------------------------|---------------------|-----------------------------|-----------------------------|--------------------------|--------|--------|----------------------------|----------|------|--------|--------|--------|
| A | TTIP1 | TTIP1 | TRING1 | RSYNC1 | TCHBLK/ CLK1 | TSIG2 | REFCLKIO | A11 | A7 | A1 | DVSS | N.C. | DVSS | N.C. | N.C. | N.C. | |
| B | ATVDD1 | ATVSS1 | TRING1 | TSYNC1 | RCHBLK/ CLK2 | RSYNC2 | MCLK | A10 | A8 | A2 | DVSS | N.C. | DVSS | N.C. | ATVSS8 | ATVDD8 | |
| C | RTIP1 | RRING1 | AL/ RSIG/ FLOS1 | RMSYNC1/ RFSYNC1 | TCLK1 | RMSYNC2/ RFSYNC2 | TCHBLK/ CLK2 | A12 | A6 | A0 | DVSS | N.C. | DVSS | N.C. | N.C. | N.C. | |
| D | ARVDD1 | ARVSS1 | RLF/ LTC1 | RSIG1 | TSIG1 | RSER2 | TCLK2 | DIGIOEN | A5 | N.C. | N.C. | DVSS | DVSS | N.C. | ARVSS8 | ARVDD8 | |
| E | ARVDD2 | ARVSS2 | RLF/ LTC2 | RCHBLK/ CLK1 | RSER1 | RSIG2 | TSER2 | BPCLK | A4 | DVSS | N.C. | N.C. | N.C. | N.C. | ARVSS7 | ARVDD7 | |
| F | RTIP2 | RRING2 | AL/ RSIG/ FLOS2 | RCLK1 | JTCLK | TSER1 | TSYNC2 | A9 | A3 | DVSS | N.C. | N.C. | N.C. | N.C. | N.C. | N.C. | |
| G | ATVDD2 | ATVSS2 | TRING2 | RCLK2 | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | N.C. | N.C. | ATVSS7 | ATVDD7 |
| H | TTIP2 | TTIP2 | TRING2 | JTDI | DVDDIO | DVDDIO | ACVDD | DVDD | DVDD | DVDDIO | DVDDIO | DVSS | DVSS | N.C. | N.C. | N.C. | |
| J | TTIP3 | TTIP3 | TRING3 | JTDO | DVSSIO | DVSSIO | ACVSS | DVSS | DVSS | DVSSIO | DVSSIO | $\overline{\text{RESETB}}$ | N.C. | N.C. | N.C. | N.C. | |
| K | ATVDD3 | ATVSS3 | TRING3 | JTMS | DVSS | DVSS | DVSS | DVSS | DVSS | DVSS | DVSS | DVSS | N.C. | N.C. | ATVSS6 | ATVDD6 | |
| L | RTIP3 | RRING3 | AL/ RSIG/ FLOS3 | RCLK3 | $\overline{\text{JTRST}}$ | RCHBLK/ CLK3 | TCHBLK/ CLK3 | TCLK4 | D1 | DVSS | DVSS | RSYSCLK | TXENABLE | N.C. | N.C. | N.C. | |
| M | ARVDD3 | ARVSS3 | RLF/ LTC3 | RCLK4 | RSIG3 | TSYNC3 | TSYNC4 | $\overline{\text{RDE}}/DSB$ | D5 | DVSS | N.C. | N.C. | BTS | N.C. | ARVSS6 | ARVDD6 | |
| N | ARVDD4 | ARVSS4 | RLF/ LTC4 | RSER3 | RSYNC3 | RSER4 | TSER4 | D0 | D6 | DVSS | DVSS | N.C. | TSSYNCIO | N.C. | ARVSS5 | ARVDD5 | |
| P | RTIP4 | RRING4 | AL/ RSIG/ FLOS4 | RMSYNC3/ RFSYNC3 | TCLK3 | RMSYNC4/ RFSYNC4 | TCHBLK/ CLK4 | D2 | N.C. | N.C. | N.C. | DVSS | TSYSCLK | N.C. | N.C. | N.C. | |
| R | ATVDD4 | ATVSS4 | TRING4 | TSER3 | RSIG4 | TSIG4 | $\overline{\text{WRB}}/RWB$ | D4 | $\overline{\text{INTB}}$ | DVSS | N.C. | DVSS | N.C. | N.C. | ATVSS5 | ATVDD5 | |
| T | TTIP4 | TTIP4 | TRING4 | TSIG3 | RCHBLK/ CLK4 | RSYNC4 | $\overline{\text{CSB}}$ | D3 | D7 | DVSS | N.C. | DVSS | N.C. | N.C. | N.C. | N.C. | |

15. PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. The package number provided for each package is a link to the latest package outline information.)

15.1 256-Ball TE-CSBGA ([56-G6028-001](#))



16. DOCUMENT REVISION HISTORY

| REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---------------|---|-------------------------|
| 102106 | New product release. | — |
| 012307 | Corrected TSYNC1 ball (from B1 to B4). | 20 |
| | Corrected RSYNC3 and RSYNC4 (previously said RSYNC2 for both). | 21 |
| | Corrected DVDD balls—previous revision stated “G5, G12” but this is “G5–G12.” | 24 |
| | Figure 8-11: In Note 4, changed S2/S3 to S3/S4 and changed S4/S5 to S5/S6; added Note 6. | 72 |
| 060607 | Added commercial temperature range devices (DS26524G and DS26524G+) to <i>Ordering Information</i> table. | 1 |
| | Added commercial temperature range to <i>Absolute Maximum Ratings</i> and added “for DS26524GN” to the temp range for Table 11-1, Table 11-3, Table 12-1, Table 12-2, Table 12-3, and Table 12-4. | 248, 250, 253, 256, 259 |
| | In Table 11-4, added commercial temperature range to Ambient Temperature. | 249 |
| 112907 | Elaborated on pin descriptions for TCLK, TCHCLK, and RCHCLK. | 20, 22 |
| | In the <i>Absolute Maximum Ratings</i> section, added GBD note for cold test (Note 1). | 248 |